MITIGATION OF TRANSIENT RADIATION EFFECTS IN ADVANCED SILICON-GERMANIUM TECHNOLOGIES

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MITIGATION OF TRANSIENT RADIATION EFFECTS IN ADVANCED SILICON-GERMANIUM TECHNOLOGIES

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To my parents José and Maria Lourenço,

whose sacrifice and unwavering support

have allowed me to be where I am today.

Mãe e Pai, muito obrigado por tudo que vocês fizeram para mim.

Eu nunca poderia ter chegado aqui sem o seu amor e ajuda.

Eu dedico esta dissertação para vocês.

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SUMMARY

The need for flexible, low-cost electronics in extreme environment applications has brought silicon-germanium (SiGe) technologies into the spotlight, but the viable long-term capabilities of these semiconductor platforms in radiation-intense environments remains largely unexplored. Conventional design methodologies for radiation-hardened electronics rely on multiple system redundancies and metallic shielding, but these solutions come at severe size, weight, and cost penalties. Accurate device models coupled with radiation event simulation techniques are necessary to provide an effective method to analyze device-level operational sensitivities and predict the circuit-level and system-level response to these random transient processes.

The potential to combine the wide-temperature performance of silicon-germanium heterojunction bipolar transistors (SiGe HBTs) with low-overhead, radiation-hardening-by-design (RHBD) techniques can enable low-cost solutions for a variety of extreme environment applications. Therefore, the objective of this research is to explore the mechanisms of transient phenomena within bulk SiGe HBTs and develop novel techniques for mitigating radiation-induced damage within these silicon-based platforms. The inverse-mode operating regime is presented as a potential method for reducing single-event sensitivities within SiGe-based, bipolar logic. Complementary (*npn* + *pnp*) SiGe BiCMOS platforms are shown to exhibit an improved radiation response due to the enhanced electrical isolation provided by *pnp* SiGe HBTs. In addition, this work will assess the efficacy of mixed-mode simulation techniques with respect to the radiation-induced transient response of SiGe-based RF circuits as well as investigate the impact of semiconductor scaling on the radiation tolerance of current and future SiGe technologies. The following is a summary of the contributions of this work:

1. An investigation into the single-event effect (SEE) sensitivity of current, state-of-the-art fourth-generation SiGe HBTs. This analysis was presented at the IEEE Nuclear and Space Radiation Effects Conference (NSREC) 2013, published in the IEEE Transactions on Nuclear Science (TNS) © 2013 [1] and in the Government Microcircuit Applications and Critical Technology Conference (GOMAC) 2015, and extends work from IEEE TNS © 2012 [2].

2. An investigation of the single-event transient (SET) response of a third-generation complementary SiGe (npn + pnp) BiCMOS platform. This work was presented at NSREC 2014 and published in IEEE TNS © 2014 [3] and in GOMAC 2015. This work was selected for the "Outstanding Student Conference Paper Award" for NSREC 2014 by the IEEE Nuclear and Plasma Physics Society (IEEE NPSS).

3. An assessment of radiation modeling strategies focused on the fidelity of mixed-mode simulations against experimental data for a SiGe L-band LNA. This work was presented at NSREC 2015 and published in IEEE TNS © 2015 [4].

4. An investigation on the impact of semiconductor scaling on the radiation-induced transient response of current and future SiGe technologies. This work has been accepted for oral presentation at NSREC 2015 and an extension is planned for publication in IEEE TNS.

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CHAPTER 1

INTRODUCTION

1.1 Origin and History of the Problem

The microelectronic revolution has brought about a paradigm shift in the way the world performs business and distributes information, leading to the ubiquitous presence of technology in day-to-day activities. While many electronic applications such as general computing and consumer electronics are designed for stable ambient conditions, there is a growing need in the aerospace, space exploration, and automotive industries for microelectronic design platforms that are robust within extreme environments. Furthermore, as applications such as global telecommunications, weather radar, and satellite navigation (GPS) incorporate advanced in-orbit electronics, it is pertinent to understand how these systems operate within a dynamic and potentially hazardous environment.

With regards to orbital and interplanetary applications, extreme environments are traditionally defined as environments with ambient temperatures outside of military specification range (mil-spec, -55 °C to 125 °C) and/or intense exposures to ionizing radiation. The lunar surface, for example, has an average surface temperature between -180 °C and 125 °C. The surface temperature of Mars is relatively cold, ranging between -143 °C to 35 °C due to its tilted axis, orbital eccentricity, and thin atmosphere. The mean surface temperature of Venus, on the other hand, is a scorching 460 °C. In addition to these extremely wide temperature ranges, these systems must endure heavy bombardment of ionizing radiation from solar, planetary, and galactic sources. Conventional design methodologies for radiation-hardened electronics rely on multiple system redundancies and metallic shielding, which come at severe size,

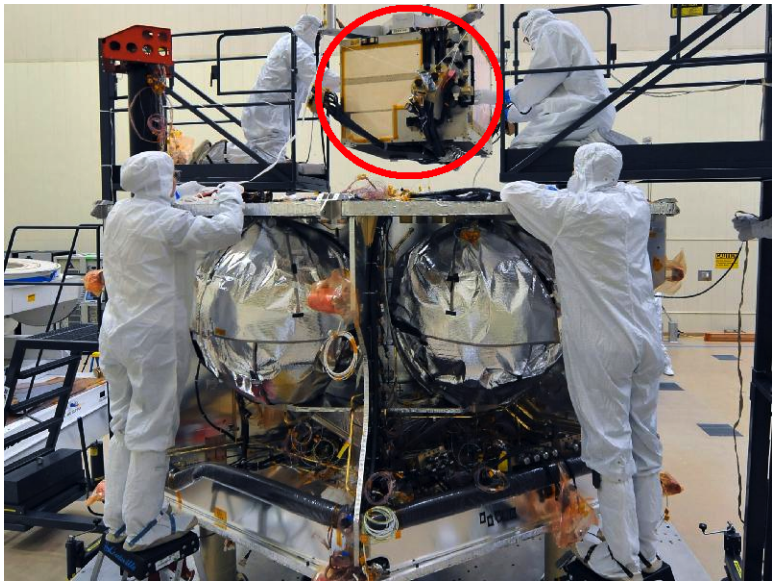


Figure 1.1: The Juno spacecraft being assembled at JPL. The radiation vault has been highlighted (courtesy of NASA).

weight and cost penalties. For example, the encircled module in Fig. 1.1 is the radiation vault used in NASA's Juno spacecraft. This protective enclosure weighed approximately 200 kilograms and shielded the Juno spacecraft's central electronics from Jupiter's harsh trapped radiation environment. Light-weight materials, such as silica aerogels and aluminum are commonly used to reduce unnecessary weight, but since present-day launch costs can be prohibitively high (e.g., $10,000 to $25,000 per kilogram to low-Earth orbit (LEO) [5]), there is a substantial interest in flexible, low-cost electronics that can tolerate unshielded exposure to these extreme conditions, leading to increased research efforts within the radiation effects community. However, the viable long-term capabilities of many silicon-based platforms within extreme environments remains largely unexplored.

1.2 Silicon-Germanium Heterojunction Bipolar Technology

For over fifty years, silicon has been the semiconductor of choice for most general-purpose electronics. During this time, bulk silicon platforms have followed the exponential growth pattern predicted by Intel co-founder Gordon Moore in 1965 [6], driving remarkable feats in digital storage and communication. However, lateral shrinking of silicon technologies is approaching a physical limit and many "vanilla" silicon processes are unable to provide the performance necessary for high-speed digital and RF communications.

As shown in Fig. 1.2, a Si BJT can be simplified as two p-n junctions placed side-by-side to create a three terminal device. From basic p-n junction physics, majority carriers diffuse from one doped region into an adjacent region of opposite doping type and vice versa. As electrons and holes diffuse across these junctions, they leave behind ionized donor or acceptor atoms (fixed positive charge in n-type silicon, fixed negative charge in p-type silicon), giving rise to depletion or space charge regions (SCRs). The fixed charge at either side of the SCR generates a built-in electric field and potential barrier that maintains charge neutrality once the system reaches equilibrium. Applying an external voltage across these junctions reduces this potential barrier, resulting in an exponential increase in carrier diffusion across the SCR. If one side (the emitter) of the p-n junction is more heavily doped, then most of this current

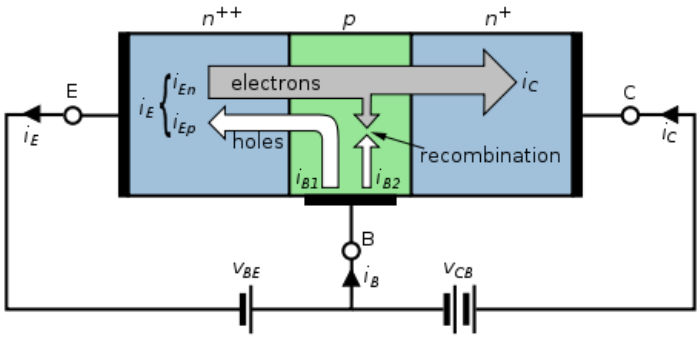


Figure 1.2: A simplified diagram of a bipolar junction transistor.

across the SCR is due to the majority carrier diffusion from the highly-doped side. Furthermore, if the lowly-doped side (the base) is made extremely thin or narrow, only a small fraction of these injected carriers will recombine in the base leaving the majority of carriers to diffuse across the base, sweep across the second SCR, and be collected at the third terminal (the collector). Therefore for a small input current into the base terminal of the transistor, a large current is driven between the emitter and collector terminals. Improving current gain in a traditional Si BJT is accomplished by manipulating the base doping profile. Since the collector current is inversely proportional to the integrated base charge (base Gummel number), it can be improved by reducing the base doping level. However, there are practical performance limitations that restrict the minimum base doping concentration since a reduction in base doping also increases the intrinsic base resistance, resulting in poor high-speed performance and higher device noise. Therefore, there is a fundamental trade off between current gain and speed/noise performance for a Si BJT.

The SiGe HBT utilizes bandgap engineering to overcome this fundamental limitation in Si homojunction BJTs. The idea of incorporating germanium into the active area of a Si BJT is not a new one, dating back to William Shockley and his original 1951 patent of the *npn* bipolar transistor [7]. Herbert Kroemer generalized the concept of the heterojunction bipolar transistor (HBT) and provided the theoretical understanding of bandgap engineering in 1957 [8]. While the theoretical framework of bandgap engineering and the HBT were in place, process engineers were unable to epitaxially grow defect-free SiGe films until the mid-1980s [9–11]. Currently, there are multiple foundries that provide high-performance silicon-germanium (SiGe) processes for the public and private sectors. IBM Microelectronics demonstrated its commercially-available, first-generation SiGe BiCMOS process (IBM 5AM) in 1992 [12] and introduced its state-of-the-art, fourth-generation SiGe BiCMOS process (IBM 9HP) in 2012 [13]. TowerJazz Semiconductor provides several generations

of SiGe processes with lithographic dimensions down to 130 nanometers [14]. The Institute of High Performance (IHP) Microelectronics currently produces the industry's fastest SiGe HBT [15] and complementary SiGe BiCMOS (C-SiGe BiCMOS) design platforms [16]. Device parameters for three representative examples of modern SiGe technologies are shown in Table 1.1.

Table 1.1: Device parameters from three modern SiGe BiCMOS technologies.

Parameter	IBM 9HP	IHP SG13G2	Jazz SBC18H3
Lithographic Node (nm)	100	130	180
Peak f_T (GHz)	300	300	240
Peak f_{MAX} (GHz)	350	500	270
BV_{CEO} (V)	1.7	1.6	1.6
BV_{CBO} (V)	5.2	5.1	5.5

The introduction of germanium into the silicon lattice lowers the effective bandgap of the material (now a SiGe alloy), which in turn reduces the potential barrier seen by electrons in the emitter and boosts carrier injection into the base. This effectively decouples the base profile design from the current gain, allowing for higher doping concentrations to lower the intrinsic base resistance and improve device speed and noise. Fig. 1.3(a) details the lateral and vertical structures of a representative first-generation SiGe HBT. The deep trench isolation helps reduce "cross-talk" between adjacent devices and allows for devices to be placed in close proximity to one another. Since the *ac* performance of a SiGe HBT is a strong function of its vertical profile, most changes between SiGe technology generations are focused on vertical profile optimizations in order to further reduce unwanted parasitics. The base doping of a Si BJT is normally around 10^{15} to 10^{16} cm^{-3}, but as shown in Fig. 1.3(b) for a first-generation SiGe HBT, the base boron doping concentration can be increased to around 10^{18} cm^{-3}, a difference of two to three orders of magnitude!

The shape of the Ge profile within the quasi-neutral base has powerful implications

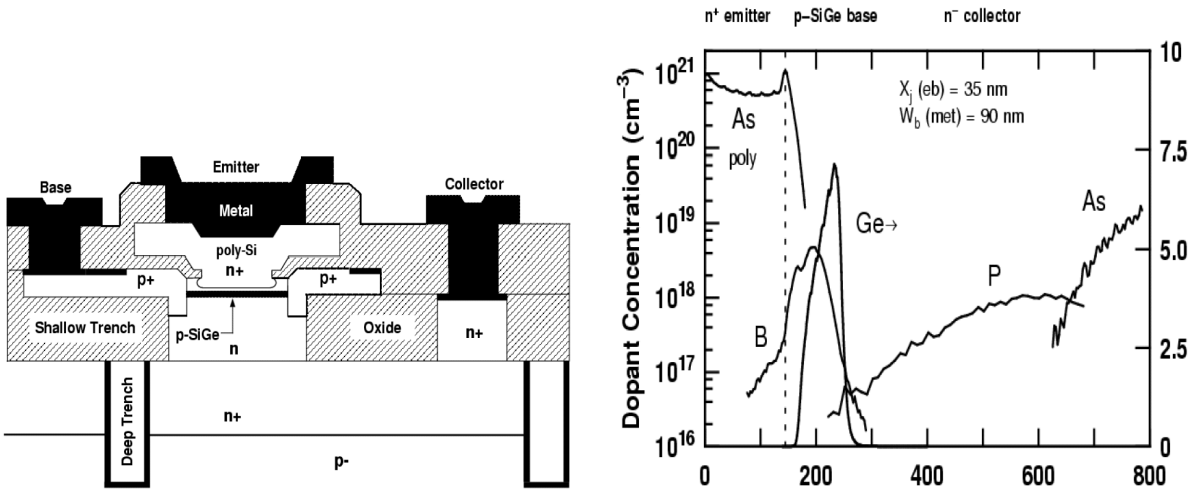


Figure 1.3: (a) Schematic cross-section and (b) measured SIMS profile of a representative first-generation SiGe HBT (after [17]).

on device performance. To simplify the following discussion, we will focus on two different types of Ge profiles that highlight distinct performance enhancements: the box (constant Ge) profile and the triangular or ramp (linearly graded Ge) profile as shown in Fig. 1.4). Both profiles have the same total Ge content, which can be visualized as the area of the box or triangular profile. By defining the Ge-induced bandgap grading factor as

$$\Delta E_{g,Ge}(grade) = \Delta E_{g,Ge}(W_b) - \Delta E_{g,Ge}(0) \tag{1.1}$$

where $\Delta E_{g,Ge}(0)$ and $\Delta E_{g,Ge}(W_b)$ are the Ge-induced reductions in the base energy bandgap at the emitter-base and collector-base edges of the quasi-neutral base, respectively. Eqns. 1.2 – 1.4 describe the improvement in current gain (β), Early voltage (V_A) and base transit time (τ_B), three important parameters that describe the *dc* and *ac* performance of a bipolar transistor, between a comparatively built SiGe HBT and Si BJT (i.e., similar doping profiles, identical emitter contact topology, etc.).

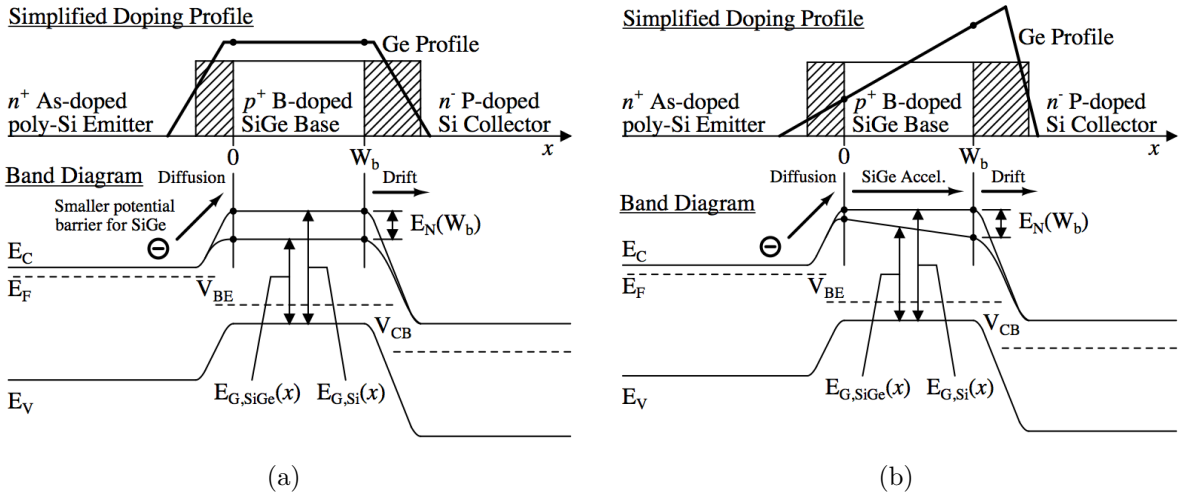


Figure 1.4: Simplified HBT schematics and energy band diagrams for a) constant (box) Ge profile and b) linearly graded (triangular or ramp) Ge profile (after [17]).

$$\left.\frac{\beta_{SiGe}}{\beta_{Si}}\right|_{V_{BE}} = \frac{\tilde{\gamma}\tilde{\eta}\Delta E_{g,Ge}(grade)/kT \; e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \tag{1.2}$$

$$\left.\frac{V_{A,SiGe}}{V_{A,Si}}\right|_{V_{BE}} \simeq e^{\Delta E_{g,Ge}(grade)/kT}\left[\frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT}\right] \tag{1.3}$$

$$\frac{\tau_{b,SiGe}}{\tau_{b,SiGe}} = \frac{2}{\tilde{\eta}}\frac{kT}{\Delta E_{g,Ge}(grade)}\left\{1 - \frac{kT}{\Delta E_{g,Ge}(grade)}\left[1 - e^{-\Delta E_{g,Ge}(grade)/kT}\right]\right\} \tag{1.4}$$

Eqn. 1.2 shows that the improvement in β is linearly proportional to the Ge-induced bandgap grading factor, $\Delta E_{g,Ge}(grade)$ and exponentially dependent on the Ge-induced band offset at the emitter-base boundary, $\Delta E_{g,Ge}(0)$. From Eqns. 1.3 and 1.4, the improvements in V_A and τ_b are dependent only upon $\Delta E_{g,Ge}(grade)$. Therefore, a box profile achieves maximum β improvement but no improvement in V_A or τ_b as there is no Ge grading across the neutral base. However, the Ge grading factor is greatest for a ramp or triangular profile so devices incorporating these types of profiles will benefit from improved V_A and τ_b, but any enhancement in current gain (β) will be reduced due to the lower Ge content at the emitter-base boundary. Hybrid

profiles such as Ge trapezoids provide improved gain while maintaining good dynamic response [17]. Both Ge profiles in Fig. 1.4 exhibit a steady decrease in Ge content near the collector-base junction, called a Ge retrograde. This Ge retrograde helps mitigate high-injection effects that may degrade device performance, most notably Kirk effect and heterojunction barrier effects (HBE). Fig. 1.5 shows the theoretical calculations for the current gain, Early voltage, and base transit time ratios as a function of Ge profile shape and confirms that a box Ge profile (i.e., % $Ge(x = 0) = 5$ and % $Ge(grade) = 0$) exhibits maximum β while a triangular Ge profile (i.e., % $Ge(x = 0) = 0$ and % $Ge(grade) = 10$) exhibits maximum V_A and minimum τ_b. These equations show that the Ge profile magnitude and shape are powerful tuning knobs for the SiGe HBT, providing the ability to tune *dc* or *ac* device performance as needed for specific applications. An important observation from Eqns. 1.2 – 1.4 is the strong dependence between the intrinsic transistor parameters and ambient temperature, specifically that the *dc* and *ac* performance of a SiGe HBT will improve as ambient temperature decreases.

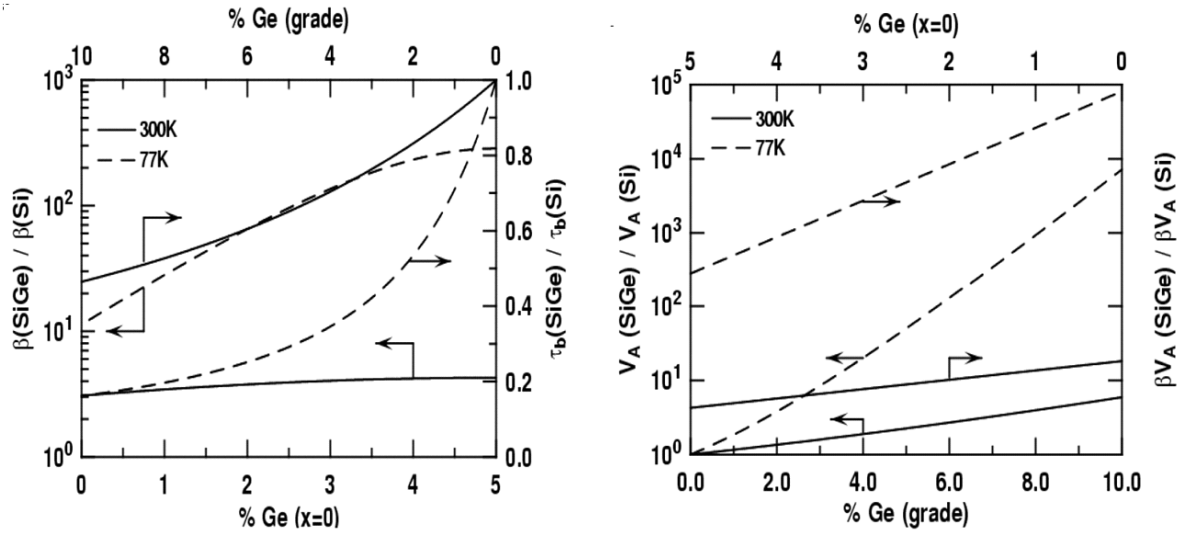


Figure 1.5: Theoretical calculations of a) the current gain (β) ratio and base transit time (τ_b) ratio; b) the Early voltage (V_A) and β-V_A product ratio as a function of Ge profile shape (after [17]).

The low-temperature capabilities of SiGe HBTs have been extensively explored. The first cryogenic investigation showed a 360% improvement in current gain (β) and a 65% improvement in unity-gain cutoff frequency (f_T) for SiGe HBTs operating at 85 Kelvin [18]. Deep-cryogenic measurements of first-generation SiGe devices and circuits have demonstrated functionality down to sub-1-K ambient temperatures [19], an impressive feat that highlights a major improvement over traditional Si BJTs. The introduction of epitaxially grown, self-aligned SiGe process flows [20,21] solidified SiGe as a viable technology for low-temperature, high-speed digital and precision analog applications [22]. Careful vertical and lateral scaling of SiGe BiCMOS platforms have incorporated larger Ge mole fractions, thinner base and collector profiles, as well as novel process innovations in an effort to reduce device parasitics and enhance performance within subsequent technology generations [13, 23, 24]. These process improvements have helped push advanced SiGe technologies into many RF/mm-wave communication [25], radar [26], and remote sensing applications [27, 28]. IHP's high-performance, 130 nm process IHP SG13-G2 (G2) represents the current performance record for *npn* SiGe HBTs at room temperature, with a unity-gain frequency (f_T) and maximum oscillation frequency (f_{MAX}) of 300 GHz and 500 GHz, respectively [29,30]. Previous work on the low-temperature operation of G2 SiGe HBTs have shown that these device exhibit exceptional performance down to 4.3 K temperatures [31]. Wide-temperature measurements of the peak transconductance (g_m) and current gain (β_{DC}) are shown in Fig. 1.6, where the *dc* performance monotonically increases with cooling. A peak g_m of approximately 0.275 mS and a β_{DC} of approximately 3,400 were observed at 4.3 K. From Fig. 1.7, extrapolated measurements of the dynamic response (i.e., f_T and f_{MAX}) show these devices exhibit a record peak f_T and f_{MAX} of 479 GHz and 798 GHz, respectively. While IHP SG13-G2 is currently the fastest, commercially-available SiGe BiCMOS process, these results coupled with semiconductor process scaling, provide indication that "THz" devices are on the horizon.

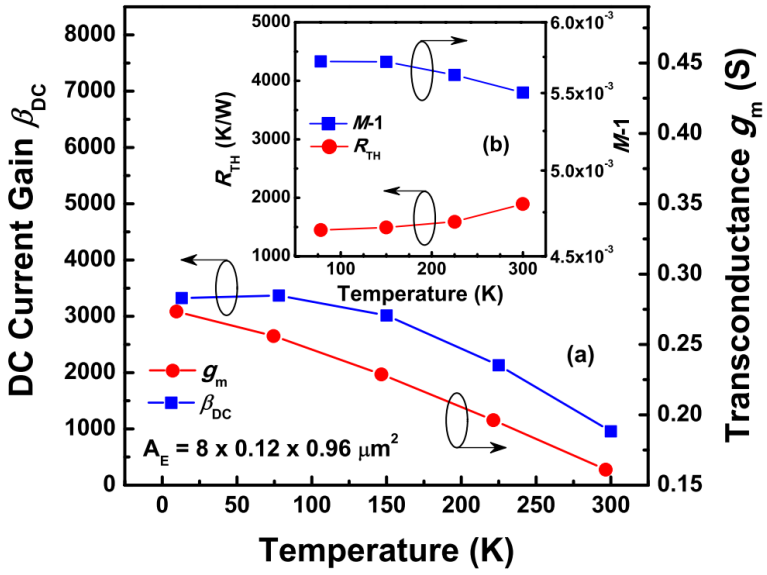


Figure 1.6: (a) Peak transconductance (g_m) and *dc* current gain (β_{DC}) as a function of temperature for the IHP G2 SiGe HBT. (b) Measured thermal resistance (R_{TH}) and avalance multiplication coefficient (M-1) at V_{CB} = 1.2 V and $J_E = 1{\times}10^{-5}$ A/μm^2 (after [31]).

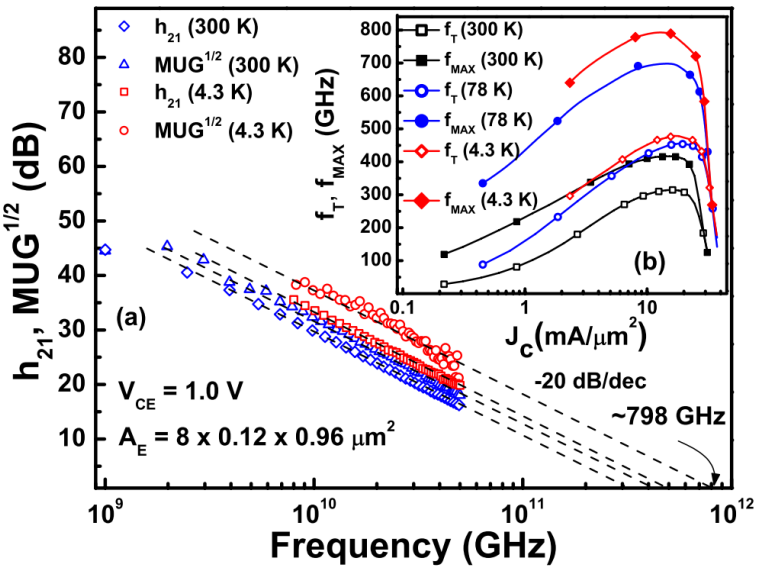


Figure 1.7: (a) Measured small-signal current gain (h_{21}) and Mason's unilateral power gain (MUG$^{1/2}$) as a function of frequency for the IHP G2 SiGe HBT at 300 K and 4.3 K. (b) Extracted unity-gain cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) as a function of collector current density (J_C) at 300 K, 78 K, and 4.3 K (after [31]).

Interest in high-temperature electronics has increased steadily over the past decade as technology improvements have begun to open up new application opportunities. An illustration detailing emerging high-temperature markets as well as semiconductor technologies and their suitable temperature ranges is shown in Fig. 1.8. The automotive industry represents one of the largest emerging markets, especially with the recent move toward hybrid and electric vehicles. Under-the-hood electronics must withstand temperatures up to 200 °C, with even higher temperatures needed for brake systems, cylinder pressure sensors, or exhaust sensing [32]. The need for more effective downhole well logging requires electronics that able to function at temperatures up to 300 °C and beyond [33]. In addition, next-generation commercial aircraft hope to reduce complexity and weight by moving control electronics closer to their respective systems, many of which are at elevated ambient temperatures [34]. Previous investigations of high-temperature reliability (i.e., ambient temperatures > 125 °C) within bulk SiGe and SiGe-on-SOI BiCMOS platforms have shown these technologies maintain adequate performance up to 300 °C (≈ 575 K) [35–37].

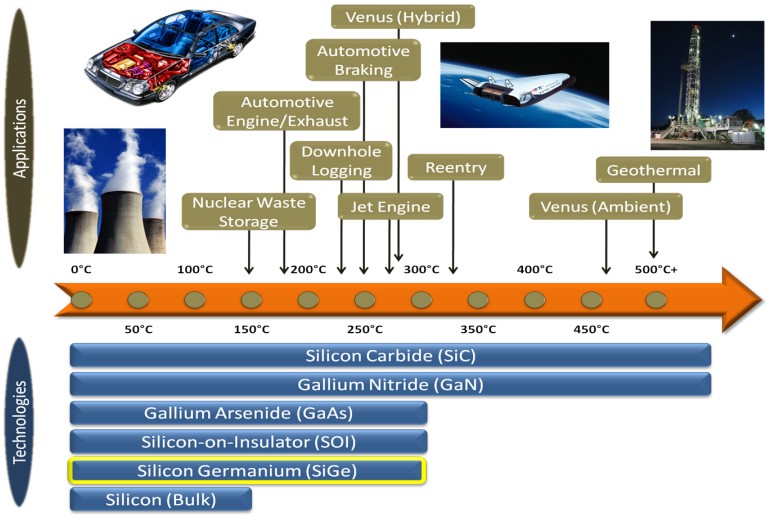


Figure 1.8: Emerging high-temperature applications and safe operating ranges of several popular semiconductor technologies.

1.3 Organization

The goal of this work is to investigate the radiation-induced transient phenomena within silicon-based platforms and demonstrate effective mitigation strategies to improve the capability of SiGe BiCMOS technologies for extreme environment applications. Chapter 2 provides an introduction to radiation effects, covering important issues in regards to semiconductor materials and electronics. Chapter 3 discusses the radiation tolerance of fourth-generation SiGe HBTs and introduces inverse-mode (IM) operation as a promising method for improving its transient response. Chapter 4 investigates the transient response of a current, state-of-the-art complementary SiGe (C-SiGe) BiCMOS process and indicates that *pnp* SiGe HBTs exhibit a superior response to high-energy radiation. Chapter 5 presents the single-event transient (SET) response of a SiGe-based, L-band low-noise amplifier (LNA), focused on accurate simulation techniques of radiation-induced effects within RF circuits. Chapter 6 investigates the radiation response across multiple SiGe technology generations and suggests that semiconductor process scaling may have a strong impact on the radiation-induced transient response of SiGe HBTs, with future SiGe technology generations potentially exhibiting increased sensitivities to single-event effects (SEE).

CHAPTER 2

INTRODUCTION TO RADIATION EFFECTS

This chapter serves as an overview on the radiation threat faced by electronics on-board satellites and spacecraft. The major sources of ionizing radiation and their effects in semiconductor materials and devices are covered, providing the background for technical discussion in future chapters.

2.1 Natural Space Radiation Environment

2.1.1 Particle Sources

Planetary satellites and deep-space spacecraft encounter a myriad of high-energy particles, the origin of which can fall into three general categories: 1) the background flux of ions originating from outside our solar system, known as galactic cosmic rays (GCRs), 2) particles emitted from the Sun during solar events, and 3) particles that are trapped by a planet's magnetic field into discrete bands (which for the Earth are known as the Van Allen belts). An artist's depiction of the natural space environment local to Earth is shown in Fig. 2.1. This radiation environment can be very dynamic, with solar activity modulating GCR fluxes and the frequency of solar events. Solar activity follows a cyclical pattern with a period of about 11 years, during which there are approximately seven years of elevated solar activity, called solar maximum, and four years where the solar activity levels are low, called solar minimum. The magnetic polarity of the Sun reverses every 11-year period, so there is a larger 22-year cycle as well. Solar activity levels are generally unaffected by the magnetic field reversal, but GCR flux models do show a correlation between the Sun's magnetic field polarity and GCR flux [38].

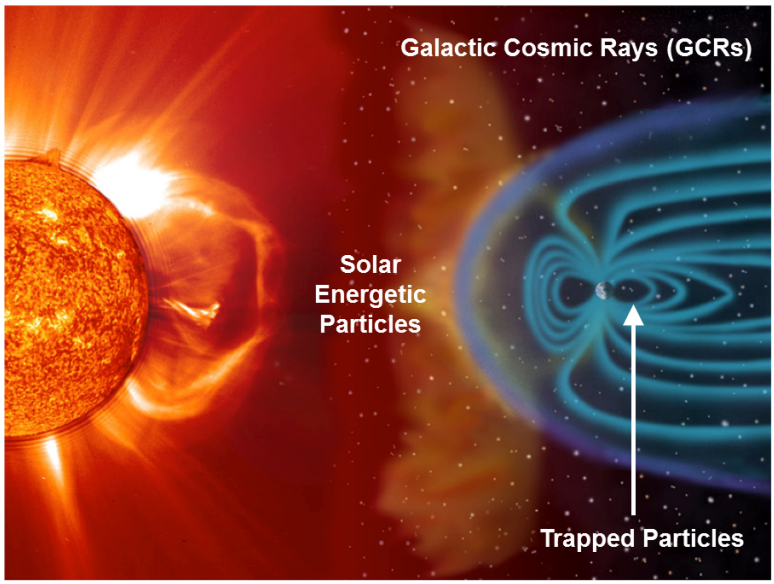


Figure 2.1: Artist's depiction of the natural space environment local to earth.

2.1.2 Galactic Cosmic Rays

GCRs originate from outside our solar system, most likely accelerated in the blast waves of supernova remnants. The particles that make up GCRs (i.e., protons, electrons, and ionized atomic nuclei) are accelerated up to a certain maximum energy from the magnetic fields within these stellar remnants. Astronomers have observed cosmic rays with energies above this maximum value and have surmised their origination to sources outside of our galaxy (e.g., active galactic nuclei) [39]. These ultra-high-energy cosmic rays (UHECRs) or extreme-energy cosmic rays (EECRs) are very rare and are not considered a part of the galactic background flux. It can be seen from Fig. 2.2 that the abundance of GCR drops off rapidly for heavy ions with nuclear charge (Z) greater than iron (Fe, Z = 26). One can logically infer this observation from the fusion processes within dying stars. As a massive star ($M_{STAR} > 10$ solar masses) begins to deplete itself of its hydrogen fuel source, it will continue to fuse heavier elements up until a core of iron is formed. The fusion of iron is an endothermic process, resulting in a sudden gravitational collapse of the star's core. Elements that are heavier than iron are fused in the high-energy densities within supernovae.

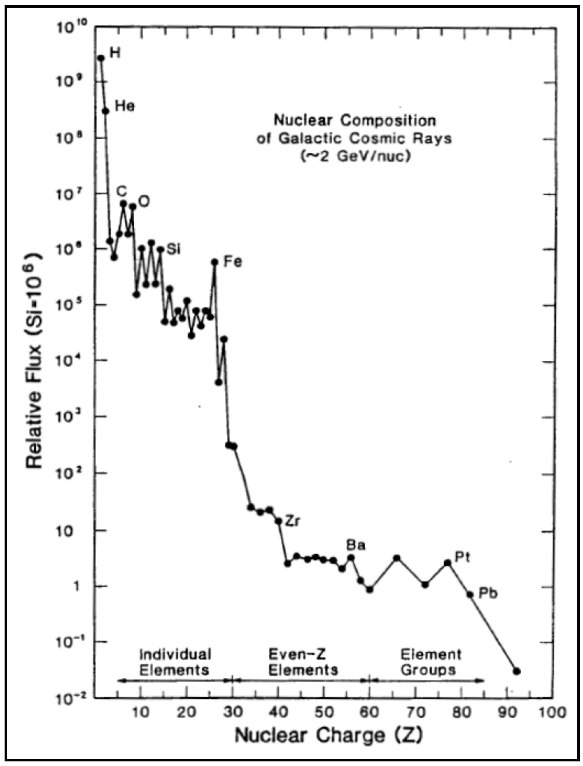


Figure 2.2: GCR relative abundances by nuclear charge (Z), normalized to silicon flux (after [40], [41]).

Table 2.1: Characteristics of Galactic Cosmic Rays (after [40]).

Hadron Composition	Energies	Flux	Radiation Effects	Metric
87% protons 12% alphas 1% heavier ions	Up to 10^{11} GeV	1 to 10 $cm^{-2}s^{-1}$	SEE	LET

Approximately one percent of stars have the mass necessary to generate supernovae, so it is not a surprise that these elements constitute a small fraction of GCRs. Some general characteristics of GCRs are shown in Table 2.1.

GCRs with energies less than 10 GeV/amu of kinetic energy are modulated by the Sun's magnetic field and solar wind. The greatest suppression occurs during solar maximum, when solar wind fluxes are at their maximum. The Sun's modulative

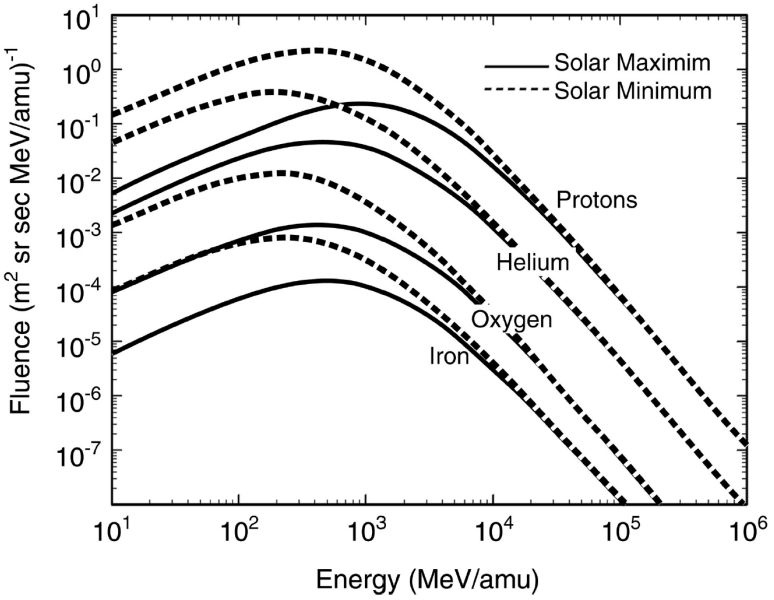


Figure 2.3: GCR energy spectra for protons, helium, oxygen and iron during solar maximum and solar minimum (after [38]).

effects on particle fluence across GCR energy are graphically shown in Fig. 2.3 for both solar minimum and solar maximum. It should be noted that several GCR models are available to the public. GCR flux models have been published by Moscow State University [42, 43] and NASA [38, 44], and an ISO standard exists (ISO 15390:2004) based on the Moscow State models.

2.1.3 Solar Energetic Particles

Solar energetic particles (SEP) are produced by two types of solar events: solar flares and coronal mass ejections (CMEs). As described in [45], solar flares result when the energy stored in the coronal magnetic field reaches a critical magnitude, generating a release of energy for a relatively short period of time (i.e., for several hours). A CME, on the other hand, is a large, long-term eruption (i.e., for a few days) of plasma, resulting in a shock wave that accelerates particles. It should be noted that CMEs are responsible for major disturbances in interplanetary space as well as major geomagnetic disturbances on Earth. Some general characteristics of CMEs are shown in Table 2.2.

Table 2.2: Characteristics of CMEs (after [40]).

Hadron Composition	Energies	Integral Fluence (>10 MeV/nuc)	Peak Flux	Radiation Effects
96.4% protons 3.5% alphas ∼0.1% heavy ions	Up to ∼GeV/nucl	$>10^9$ cm^{-2}	$>10^5$ cm^{-2}s^{-1}	TID DDD SEE

While CMEs are composed of a cocktail of different particles, protons account for about 96% of the total composition. These low and high-energy protons can cause permanent damage in the form of Displacement Damage Dose (DDD) and Total Ionizing Dose (TID). In addition, all constituent particles can cause transient and permanent single-event effects (SEE). Fig. 2.4 and Fig. 2.5 illustrate the periodic dependence of low-energy (> 0.88 MeV) and high-energy (> 92.5 MeV) protons, respectively. Attention should be focused on the statistical nature of solar particle events. Due to their stochastic nature, modeling solar particle events can be a difficult process. Luckily several models have been created, including the JPL91 [46] and ESP [47, 48] models. An additional model, known as the PSYCHIC model has been developed as an extension of the ESP model [49].

2.1.4 The Earth's Trapped Radiation Environment

The Earth's magnetosphere consists of both an external and internal magnetic field. The external field is the result of the ionized gas particles that comprise the solar wind. Earth's geomagnetic field originates from electrical currents present in the liquid outer core. The geomagnetic field can be approximated as a dipole magnet up to altitudes of about 5 Earth radii. This dipole approximation is visualized in Fig. 2.6. This dipole field is tilted about 11° from the Earth's north-south axis and displaced by more than 500 km from the Earth's geocenter [50]. The magnetic field strength is at a minimum at the magnetic equator and at a maximum at the magnetic poles.

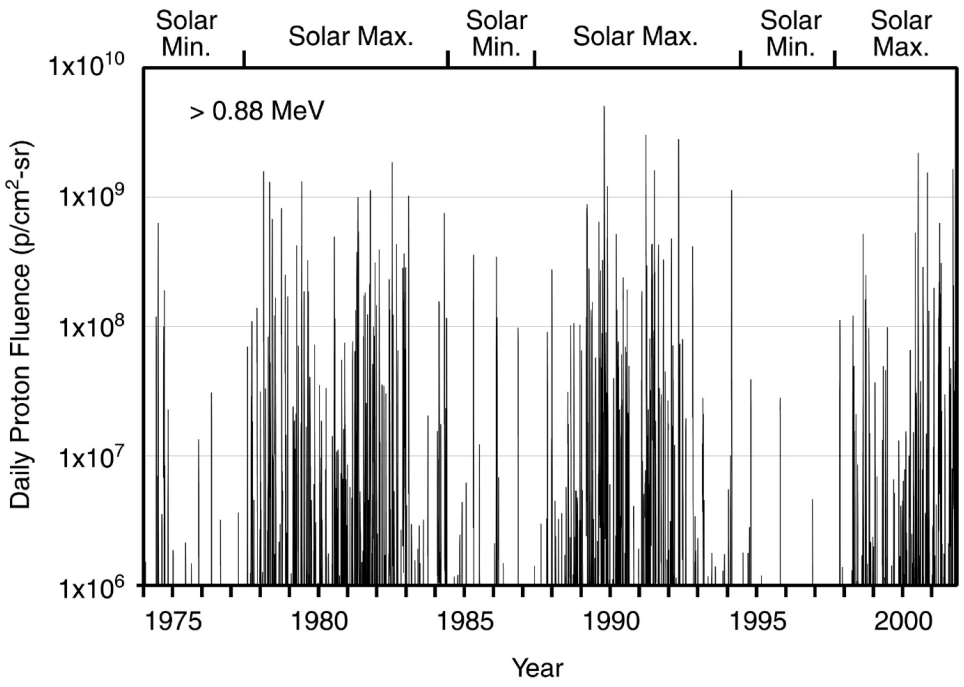


Figure 2.4: Daily fluences of low-energy (> 0.88 MeV) protons due to solar particle events between approximately 1974 and 2002 (after [40]).

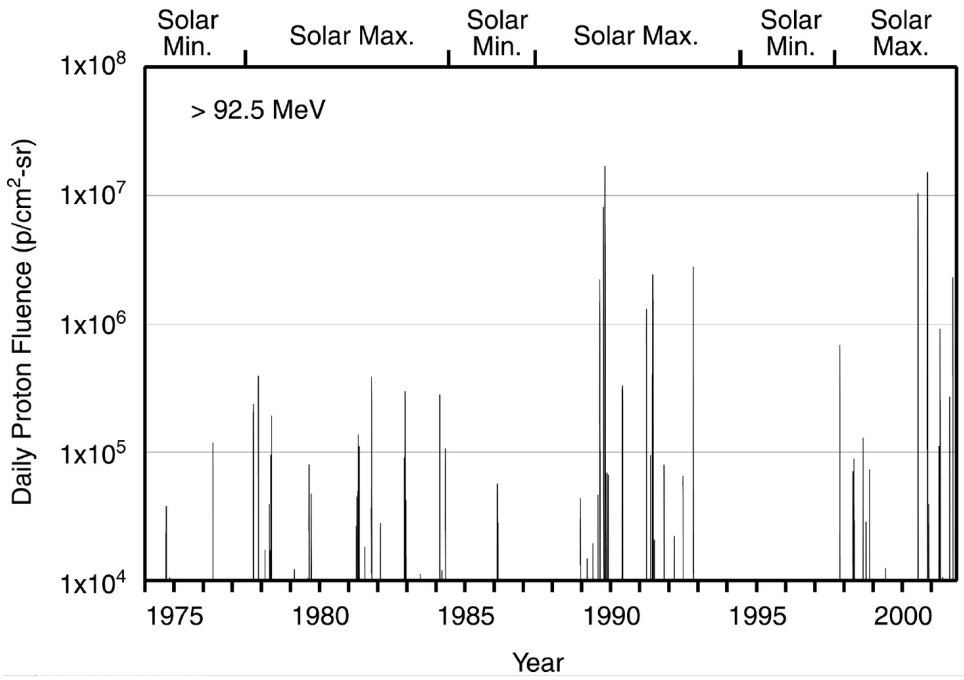


Figure 2.5: Daily fluences of high-energy (> 92.5 MeV) protons due to solar particle events between approximately 1974 and 2002 (after [40]).

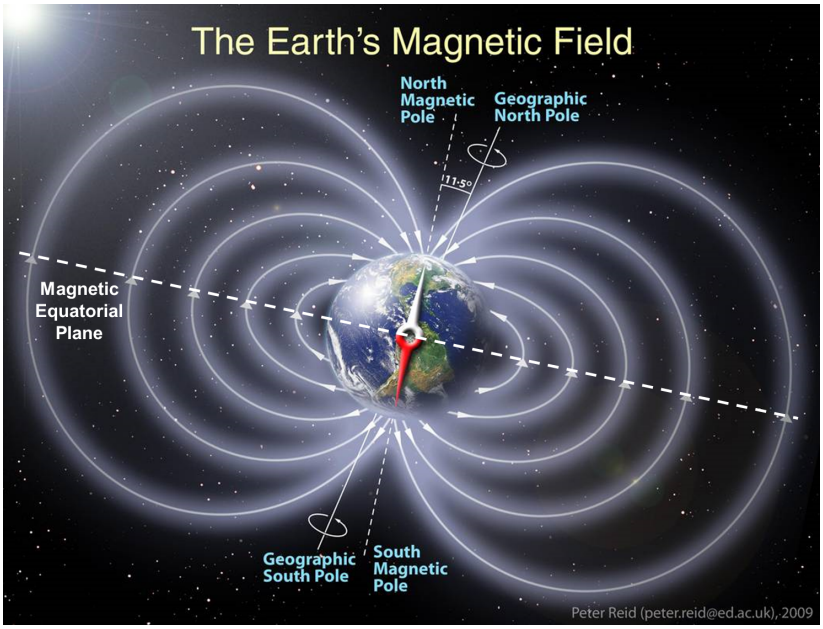


Figure 2.6: The internal magnetic field of the Earth can be approximated as a dipole field. A line symbolizing the magnetic equatorial plane has been included (courtesy of Peter Reid, The University of Edinburgh).

The McIlwain L-parameter or "L-value/L-shell" is a common parameter used to describe planetary magnetic fields [51]. L-shells are normalized to the radius of the Earth ($\approx$ 6,370 km), so an L-shell of two corresponds to a set of magnetic field lines that cross the magnetic equatorial plane at a distance of two earth radii. Similarly, field lines with an L-shell of five would cross the magnetic equatorial plane at a distance of five earth radii. L-shells are normalized to a specific planetary body and therefore can be translated to different trapped radiation environments (e.g., the Jovian environment). Protons and electrons can become trapped along these magnetic field lines, where they drift around the Earth while being dragged in the longitudinal direction. The resulting toroidal surfaces traced out by these particles are called drift shells.

Charged particle motion along the Van Allen belts is shown in Fig. 2.7. Trapped particles spiral around and move along the magnetic field lines. When the particle approaches the polar regions, the magnetic field strength increases, causing the spiral

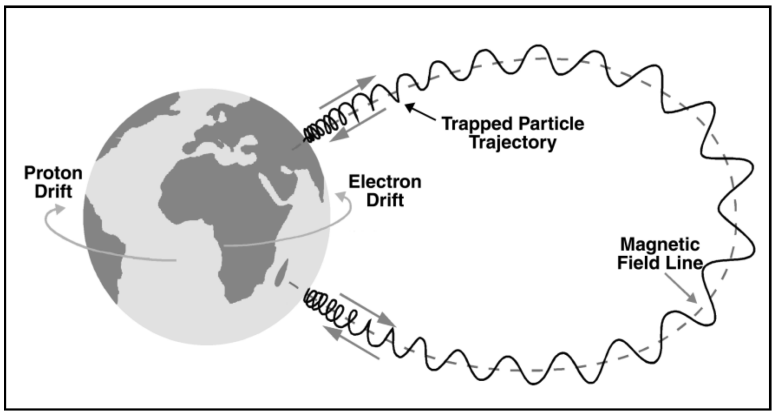


Figure 2.7: Motion of a charged trapped particle in the Earth's magnetic field (after [52]).

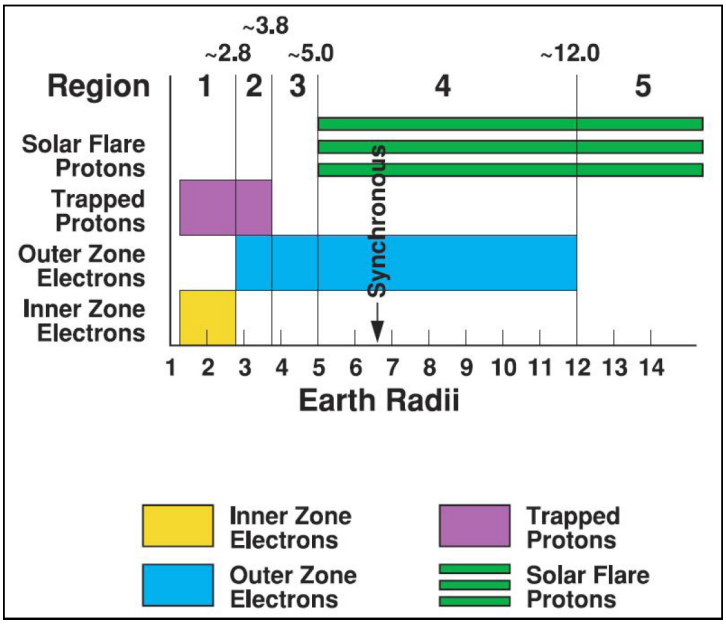


Figure 2.8: The distribution of charged particles (protons and electrons) in the Earth's magnetosphere (after [52]).

to tighten. The magnetic field continues to increase until there is sufficient force to send the particle in the reverse direction. The points where particles reflect to and fro are called "mirror points" or "conjugate mirror points." As shown in Fig. 2.7, protons and electrons longitudinally drift in opposite directions.

Fig. 2.8 shows the distribution of charged particles in the Earth's magnetosphere. Trapped protons have energies up to 100s of MeV and exist in L-shells between

1.15 and 10, though high-energy protons (> 10 MeV) only exist below altitudes of about 20,000 km (L ≈ 3.14) [45, 53]. Close to the inner edge of the Van Allen belts, proton fluxes are largely modulated by atmospheric density. At solar maximum, these proton fluxes can decrease by a factor of two to three due to atmospheric expansion and various scattering processes. Various trapped proton models have been developed and are available to the general public, including the AP-8 [54], CRRESPRO [55], and a more recent model based on SAMPEX/PET data [56].

A unique feature of the trapped proton environment is a region known as the "South Atlantic Anomaly" (SAA). Fig. 2.9 shows a cross-sectional view (cut through the Earth at meridian 325°) and flux plot highlighting the SAA. Located off the coast of Brazil, the SAA is a distinct area on the Earth where part of the inner trapped proton belt is at a lower altitude than normal. This phenomenon is caused by the tilt and displacement of the geomagnetic field with respect to Earth's axis of rotation. The SAA primarily can affect satellites and spacecraft with orbits below 1,000 km.

The trapped electron environment is unique due to the existence of two distinct zones: an inner belt with L-shells between 1 and 2.8 and an outer belt with L-shells between 2.8 and 10. Electrons in the inner zone have energies up to 4.5 MeV with peak

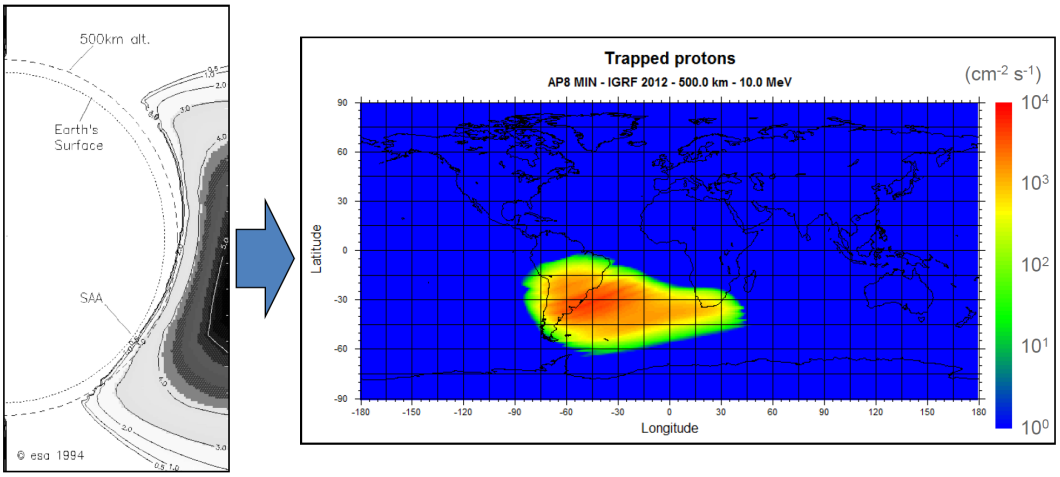
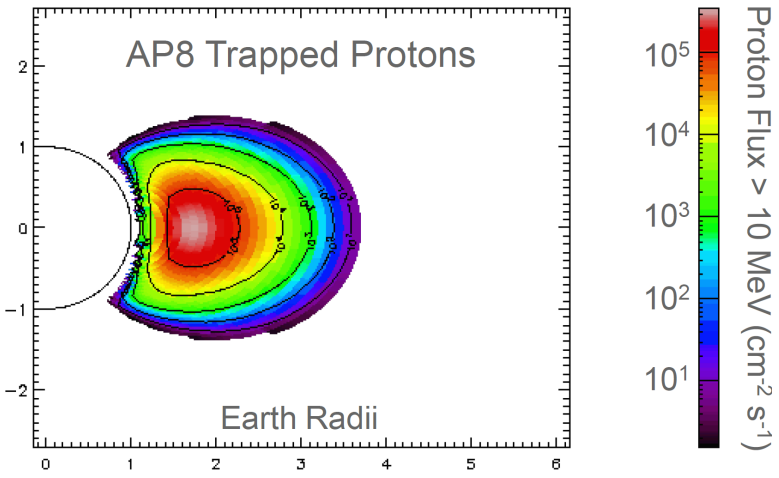


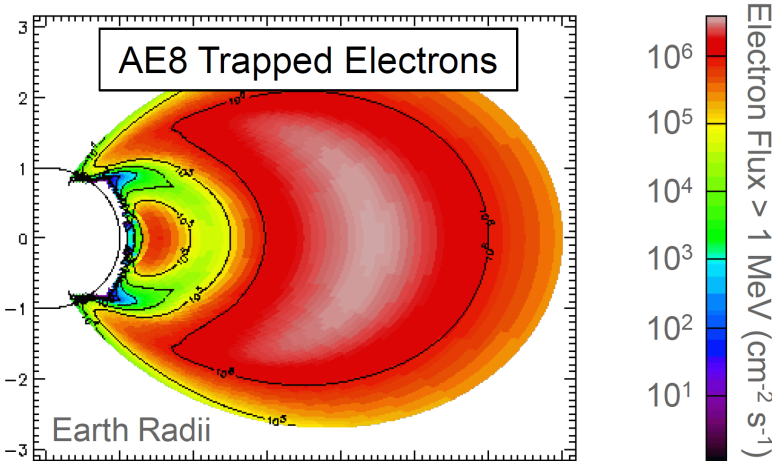
Figure 2.9: Cross-sectional view and OMERE trapped proton (10 MeV AP-8 protons at 500 km altitude) plot highlighting the "South Atlantic Anomaly" (after [50, 53]).

fluxes near L = 1.5. Inner zone electron fluxes are generally stable but can gradually increase by a factor of two or three at solar maximum. Outer zone electrons have energies that peak at about 10 MeV with peak fluxes between L = 4.0 and L = 4.5. The outer zone is very dynamic with day-to-day fluxes varying by several orders of magnitude. A long-term average value of flux for > 1 MeV electrons is approximately 3×10^6 $cm^{-2}s^{-1}$. Trapped electrons are distributed across the inner zone and outer zones, but there is a region between the high intensity zones where electron flux is at a minimum called the slot region. Due to the dynamic nature of the outer zone, the location of the slot region is dynamic but is usually between L = 2 and L = 3. There are several available trapped electron models, including AE-8 [57], CRRESELE [58], and IGE-2006/POLE [59–61]. It should be noted that all trapped proton and electron models introduced are specific to the Earth trapped particle environment. References and models for other trapped environments, including the Jovian system are also available [62].

Standalone radiation effects software and online toolsets are available for characterizing the Earth's trapped particle environment. OMERE, developed by Tests and Radiations (TRAD), is a freeware dedicated to space environment and radiation effects on electronic devices [63]. OMERE combines GCR, SEP, and trapped particle models and radiation effects analyses (DDD, TID, SEE) to provide an all-in-one interface for investigating potential reliability issues for Earth-orbiting spacecraft. The topographical map highlighting the SAA in Fig. 2.9 was generated using OMERE. The Space Environment Information System (SPENVIS) provides similar functionality, but uses an online interface for analyzing radiation effects [56,64]. Fig. 2.10 shows the trapped proton and trapped electron flux populations which were generated using the SPENVIS toolsets. The inner and outer trapped electrons zones as well as the slot region ($L \approx 2$) are visible.



(a)



(b)

Figure 2.10: Trapped particle flux populations for (a) protons with energies >10 MeV and (b) electrons with energies >1 MeV (after [53]).

2.1.5 Radiation Environment Threats

Table 2.3 lists the major constituents of the ambient radiation environment for several classes of orbital trajectories. The difference between equatorial and polar low Earth orbits (LEO) is attributed to the enhanced displacement of the Van Allen belts at the Earth's equator. Medium Earth orbits (MEO) encompass the maximum flux regions of the proton and inner electron belts, so spacecraft at these orbits are very susceptible to proton and electron damage. Geosynchronous orbits (GEO) and high Earth orbits (HEO) exist within the outer electron belt, but due to the dynamic nature of this

Table 2.3: Radiation Threat Summary (after [53], K.A. LaBel, NASA/GSFC).

Orbit	Trapped Electrons	Trapped Protons	SEPs	GCRs
LEO Low Inc.	Moderate	Yes	No	Moderate
LEO Polar	Moderate	Yes	Yes	Yes
MEO	Severe	Severe	Yes	Yes
HEO	Yes	Yes	Yes	Yes
GEO	Severe	No	Yes	Yes

region, it can be hard to predict TID/SEE at these orbits. LEO polar, MEO, GEO, and HEO are susceptible to SEPs and GCRs, while LEO with low inclination benefit from the protection of the Earth's magnetic field. Interplanetary orbits are susceptible to other planets' trapped radiation environments in addition to SEPs and GCRs.

2.2 Energy Deposition in Materials and its Effects

The mechanisms by which different types of radiation interact with matter vary, but at the basic level, high-energy particles and photons deposit energy while passing through matter. For semiconductor materials, this deposited energy manifests itself as electron/hole pairs and atomic (lattice) dislocations. The radiation type, energy, and length of exposure can have profound impact on the measured results. The following subsections will focus on electron-hole pair generation as they are the source of TID and SEE. While certainly relevant to radiation effects, DDD will not be covered in the subsequent sections. There are excellent background references covering the subject of DDD, including [65–67]. The following sections will consist of broad overviews of the mechanisms of energy deposition in matter and their effects in electronic devices (i.e., TID and SEE).

Electrons, protons, and heavy ions deposit energy into materials through two processes: direct and indirect ionization. As a charged particle passes through matter, it interacts with the field of electrons through Coulombic forces. Most interactions involve relatively small amounts of energy loss (usually a few eV) by the moving

charged particle, but enough energy is imparted to generate electron/hole pairs. There are many thousands of these "direct" ionization events along the path of a charged particle. Occasionally, a larger energy transfer may occur between the charged particle and an electron, producing an energetic secondary electron often referred to as a delta ray (δ-ray). These δ-rays will then go on to produce multiple ionization events.

A popular way to quantify direct ionization effects in matter is the linear energy transfer or LET. LET describes the amount of energy an ionizing particle has lost per unit path length through a specified material. LET has units of Energy-Length^2/Mass, commonly expressed as MeV-cm^2/mg. LET is derived by normalizing electronic stopping power, denoted as S, by the specified material density (see Eqn. 2.1).

$$LET = \frac{S}{\rho} = \frac{-dE/dx}{\rho} = \frac{MeV/cm}{mg/cm^3} = \frac{MeVcm^2}{mg} \tag{2.1}$$

Active regions of devices (e.g., the depleted channel between source and drain in a FET or the vertical bipolar region of a HBT) are often modeled as a rectangular parallelepiped (RPP). These RPP models are commonly used in SEE predictions for electronics in radiation-intensive environments. A modified LET term, called effective LET, takes into account the incidence angle of an ionized particle. Effective LET is the exact same as LET except that it is scaled by $1/\cos(\theta)$, where θ is the incident angle of the ion with respect to normal incidence. This scaling factor accounts for the increase in path length through the assumed sensitive volume (RPP). However, it should be noted that RPP models tend to form poor approximations for some bipolar technologies (e.g., SiGe HBTs) since amplification of collected charge is not taken into account.

Fig. 2.11 shows the depth in silicon (in μm) versus LET for a variety of heavy-ion particles. High-energy particles are slowed down as they traverse through matter and deposit energy. The rate of energy deposition increases as the particle slows down

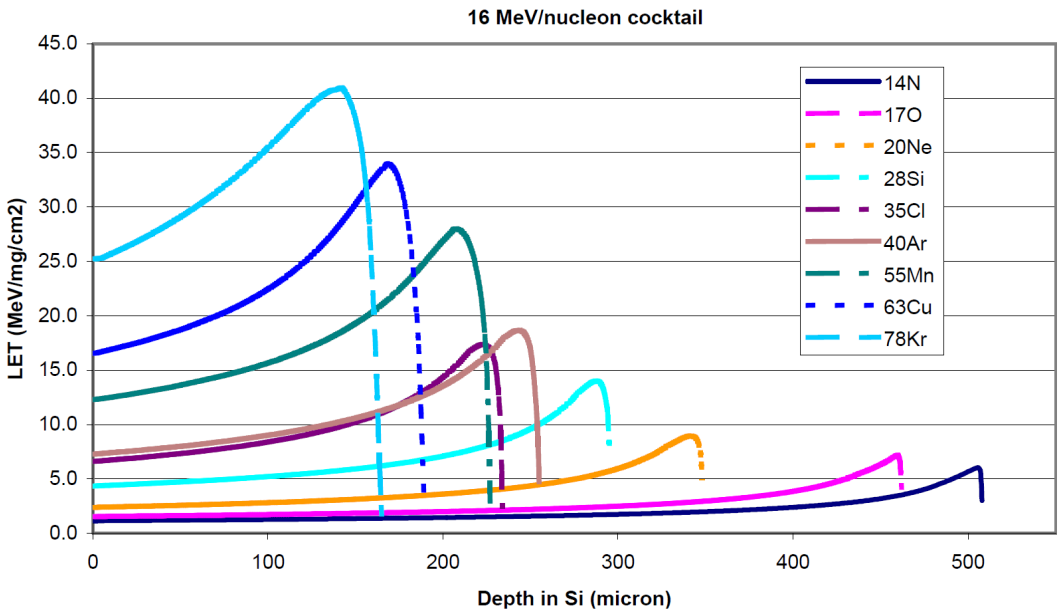
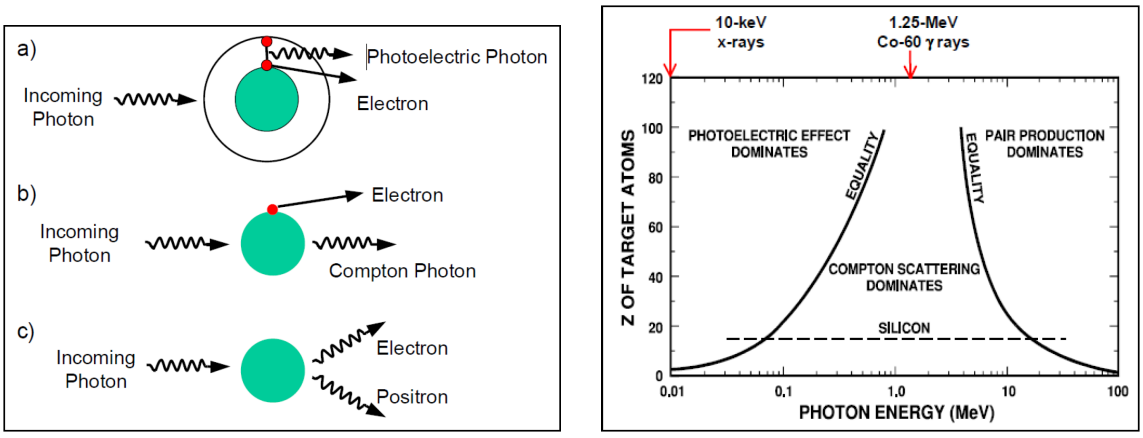


Figure 2.11: Depth in silicon (in μm) against LET (MeV-cm^2/mg) for various heavy-ions (after [68]).

until it reaches a maximum known as the Bragg peak. The particle comes to a halt shortly after the Bragg peak, resulting in a sharp drop in LET. If the energy per nucleon for all ions is fixed, heavier ions will traverse less material before halting due to greater interactions with the surrounding material. This phenomenon can result in SEE testing issues for technologies with large back-end-of-the-line (BEOL) metal stacks because the particles will exhaust most of their energy before striking the sensitive volume. Luckily, tools have been developed to help predict the energy losses for high-energy particles as they propagate through matter. SRIM/TRIM, short for Stopping and Range of Ions in Matter/Transport of Ions in Matter, are a group of free programs which calculate the transport properties of ions through matter [69]. SRIM/TRIM can generate semiconductor/insulator/metal stacks and predict LET energies at a specified depth.

Much like electrons, protons, and heavy ions, photons deposit energy within materials. However, the photons themselves cause little damage. There are three photon



(a) (b)

Figure 2.12: (a) The three photon interaction mechanisms [70] (b) Dominant photon interaction mechanism as a function of photon energy and the target atom's nuclear charge [71]; after J. R. Schwank, *et al.*

interaction mechanisms: the photoelectric effect, Compton scattering, and pair production which are illustrated in Fig. 2.12(a). All three interaction mechanisms result in the generation of an energetic secondary electron (δ-ray) that in turn creates electron/hole pairs through ionization events. In the photoelectric effect, a photon is completely absorbed by an atom, exciting an inner shell atomic electron to a high enough energy state that it is emitted from the atom. An outer shell electron then falls in to take the place of the ejected electron (photoelectron), releasing its excess energy in the form of a photoelectric photon.

Compton scattering is a type of inelastic scattering that X-rays and γ-rays undergo in matter. Compton scattering is named after Arthur Holly Compton who won the 1927 Nobel Prize in Physics for its discovery. An unexplainable phenomenon occurred when high-energy photons (X-rays) interacted with atoms. These photons were scattered through an angle θ and emerged at a different wavelength related to this scattering angle. Classical electromagnetism predicted the wavelength of scattered X-rays to remain unchanged, but experimental results revealed the scattered rays had longer wavelengths (i.e., lower photon energies). In Compton scattering,

part of the energy of the incoming photon is transferred to a scattering electron, which recoils and is ejected from the atom. The rest of the energy is taken by the scattered photon, resulting in a wavelength shift.

Pair production occurs when a high-energy photon interacts with the nucleus of an atom. The result is the creation of an electron and its anti-particle, a positron. The energy of the incoming photon is converted to mass through Einstein's mass-energy relation, $E = mc^2$, where E is the photon energy, m is the sum of the electron and positron rest masses (2× electron rest mass), and c is the speed of light. For pair production to occur, the photon must have enough energy to create the rest masses of the electron and positron. The rest mass of an electron (or positron) is about 9.11×10^{-31} kg, which translates to approximately 0.511 MeV/c^2. Fig. 2.12(b) indicates which interaction process dominates with respect to the nuclear charge of the target atom and photon energy. The dashed line at a nuclear charge of 14 (Z = 14) represents silicon and indicates that lower energy photons (e.g., 10-keV X-rays from an ARACOR X-ray irradiator) usually produce electron/hole pairs via the photoelectric effect but high-energy photons (e.g., 1.25-MeV γ-rays from ^{60}Co) will produce electrons via Compton scattering.

The use of X-rays and γ-rays for accelerated TID testing has several advantages over particle beam experiments. Photon-based testing facilities do not require the particle accelerators needed to accelerate particles with mass to high energies. Particle accelerators are complex systems that are expensive to install and costly to upkeep. Fig. 2.13 shows the fractional hole yield versus electric field in in SiO_2 for a variety of particles spanning LET. From Fig. 2.13, ^{60}Co (γ-ray) and 10-keV X-rays have high fractional hole yields, reducing exposure times and experiment costs for the end user. A key advantage between photon and proton/neutron beam facilities is the unwanted activation of devices under test (DUTs) and other testing equipment. Proton or neutron activation is a process where atoms pick up free protons or neutrons and

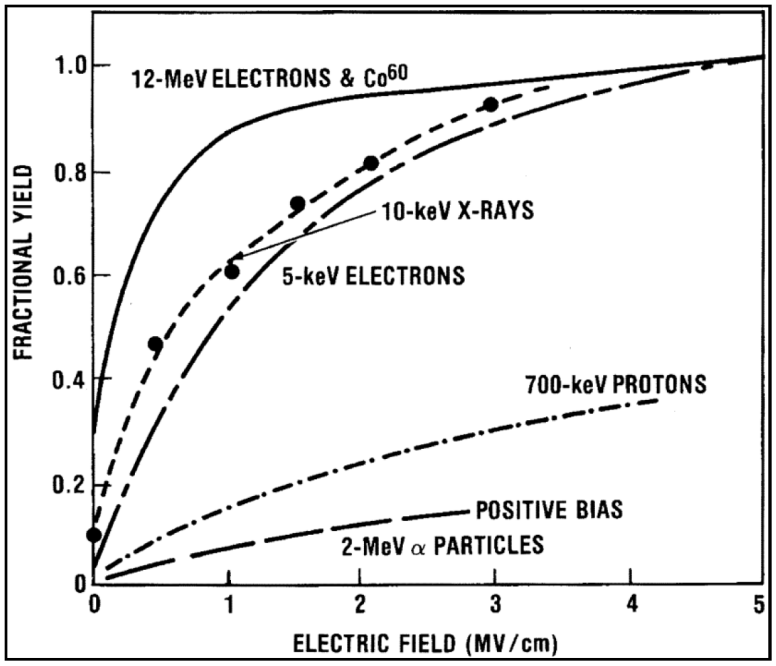


Figure 2.13: Fractional hole yield vs. electric field for various types of ionizing radiation (after [71]).

enter excited states. These excited atoms are unstable and undergo radioactive decay, which can take several days to weeks before dropping below background radiation levels. Metals, such as copper and gold, are very susceptible to proton activation. Therefore, test packages (e.g., dual in-line packages (DIPs)) and testing boards (e.g., printed circuit boards (PCBs)) may become unsafe to handle if exposed to multi-Mrad proton doses. X-ray and γ-ray tests are not without their own disadvantages. TID experienced by spacecraft is primarily a result of long-term exposure to trapped and solar protons and/or electrons, so photon-based TID testing may not accurately predict how electronics degrade over time in the natural space environment (i.e., photons do not cause DDD).

2.2.1 Total Ionizing Dose

TID is a measure of the absorbed energy from ionizing radiation in a given material. It should not be confused with the concept of equivalent, effective, or committed dose, which represent the stochastic biological effects of ionizing radiation and are reported

in sieverts or roentgen equivalent man (rem). The units of TID are equal to the energy deposited per unit mass of medium and can either be represented by the SI unit, gray (1 Gy = 1 J/kg) or the CGS unit, rad (1 rad = 100 erg/g), where 1 Gy = 100 rad. It should be noted that the rad is more commonplace in the radiation effects community and will be the unit of choice for subsequent discussions.

For advanced electronics, TID effects manifest as damage-induced parametric shifts, including threshold voltage shifts, increased off-state leakage, parasitic leakage paths, mobility degradation, and changes in recombination behavior. These shifts are primarily caused by charge trapping within bulk semiconductor and oxides or by traps generated at semiconductor/oxide interfaces. Holes are responsible for TID charge trapping and the resulting trap states because hole mobility $\ll$ electron mobility in SiO_2 [72]. For MOS devices, charge trapping in the gate oxide generates threshold voltage shifts, while charge trapping at the shallow trench isolation (STI) oxide interface creates parasitic leakage paths that increase off-state leakage. For SiGe HBTs, TID results in interface trap states at either the EB spacer oxide or STI oxide interfaces which can impact forward-mode or inverse-mode performance. This increased trap density generates a perimeter dependent space-charge generation/recombination (G/R) base leakage component, resulting in a degradation in current gain [73]. These oxide interface traps can also degrade carrier mobility and transit times, which may affect the dynamic performance of SiGe HBTs (e.g., f_T).

Table 2.4: Electron/Hole Pair Generation Energies and Pair Densities Generated by 1 rad (after [53, 71]).

Material	$\boldsymbol{E_p}$ **(eV)**	**Density** $\mathbf{(g/cm^3)}$	**Pair Density Generated per rad** $\mathbf{g_0}$, $\mathbf{(g/cm^3)}$
GaAs	4.8 (approx)	5.32	7×10^{13} (approx)
Silicon	3.6	2.328	4×10^{13}
Silicon Dioxide	17	2.2	8.1×10^{12}

In space radiation environments, TID is primarily the result of long-term exposure to trapped and/or solar protons and electrons. The amount of damage due to ionization from electrons, ions, or photons is directly proportional to the charge yield per unit dose, which is the number of electron/hole pairs generated per rad. Table. 2.4 lists several important TID parameters for various materials. E_p is the average ionization energy needed to generate an electron/hole pair and g_0 is calculated by multiplying 1 rad (100 erg/g = 6.24×10^{13}eV/g) by the material density and dividing by E_p. The actual charge yield in a given material is a function of the electric field and density of the electron/hole pairs. The large variance between particles in Fig. 2.13 indicates a strong dependence between charge yield and TID.

A schematic energy band diagram for a MOS structure is shown in Fig. 2.14, highlighting the major physical processes underlying TID response. Ionizing radiation generates electron/hole pairs which may recombine or separate depending on the device structure and biasing. Holes that do not recombine remain relatively immobile and stay near their point of generation while electrons, due to their high mobility,

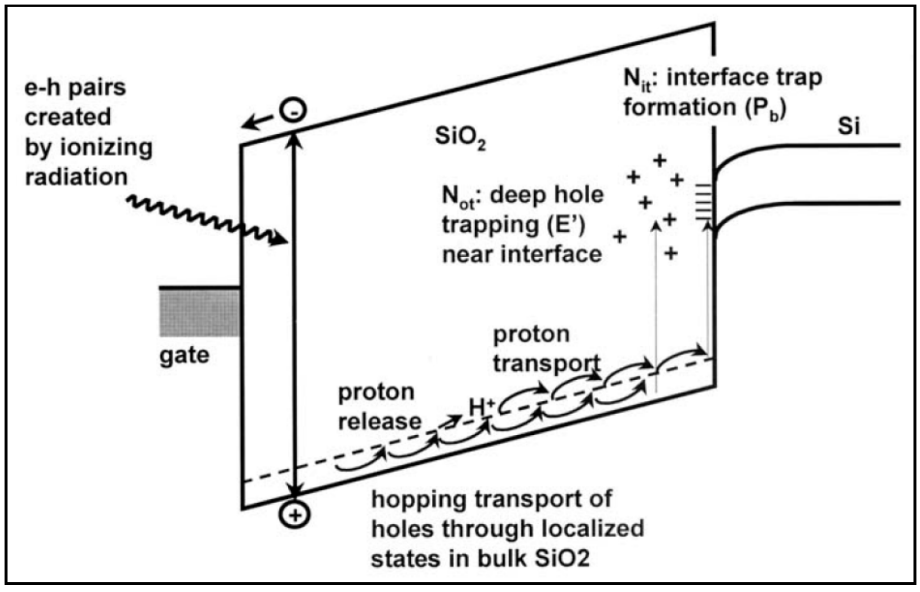


Figure 2.14: The major physical processes underlying total ionizing dose (TID) degradation (after [71, 74]).

easily escape the material. Holes gradually move towards the Si/SiO_2 interface over many decades in time (with respect to electron/hole generation times). This hopping transport process is very sensitive to temperature, oxide thickness, oxide quality, and applied field. At room temperature, this transport process is normally over in much less than one second. As the holes reach the SiO_2 interface, a fraction of them fall into deep, long-lived trap states. These states undergo gradual annealing that can be accelerated at high temperatures. In response to the fixed charge at the SiO_2 boundary of the oxide/semiconductor interface, interface traps (localized states with energy levels in the Si bandgap) build up on the silicon side, degrading device performance.

Dose rate sensitivities and enhanced low dose rate sensitivity (ELDRS) are subjects of interest within the radiation effects community. ELDRS, a radiation effect unique to bipolar technologies, is a dramatic increase in total dose degradation for DUTs exposed in low dose rate environments [76]. The effects of ELDRS on LM111 voltage comparators are shown in Fig. 2.15. Traditionally, TID characterization utilizes high dose rates to minimize experimental complexity and test time (cost) at

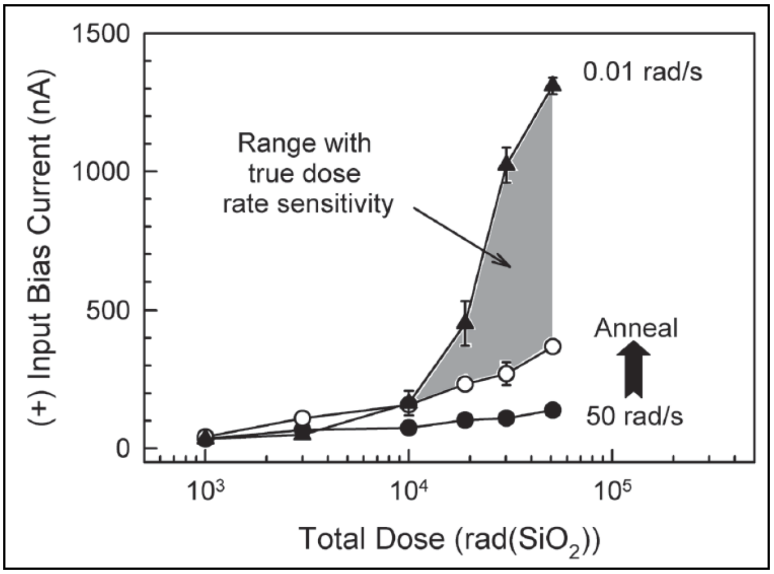


Figure 2.15: Input bias current vs. total dose for LM111 voltage comparators, highlighting ELDRS effects (after [75]).

irradiation facilities. However, the natural space environment is a low dose rate environment where total dose degradation occurs due to long-term exposures to ionizing radiation, which makes ELDRS a possible concern for orbital and deep-space missions.

Recent work across multiple generations of SiGe BiCMOS technologies have shown that SiGe HBTs are inherently immune to dose rate effects [77]. Since ELDRS is primarily observed in lateral or substrate *pnp* devices, the enhanced tolerance exhibited by SiGe HBTs over traditional Si technologies is attributed to the vertical topology of the SiGe HBT. This structure isolates the intrinsic device volume (i.e., region where carrier transport occurs) from sensitive areas, such as the shallow trench isolation region (STI region).

2.2.2 Single-Event Effects

A SEE is a disturbance to the normal operation of a circuit caused by the passage of a single ion through or near a sensitive node in the circuit. There are two major categories of SEE: destructive and non-destructive. Destructive SEE include single-event latchup (SEL), single-event burnout (SEB) and single-event gate rupture (SEGR). Non-destructive SEE include single-event upsets (SEUs), multiple bit upsets (MBUs),

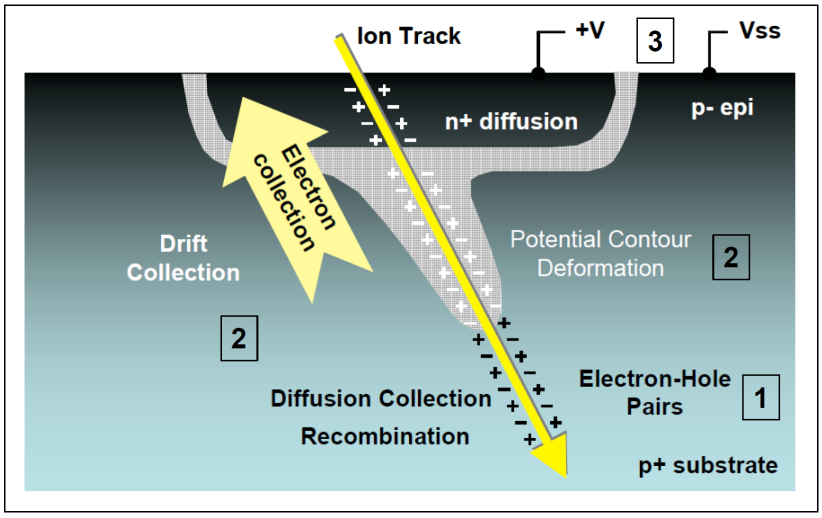


Figure 2.16: Illustration of a heavy-ion strike and the subsequent charge collection processes (after [78]).

single-event transients (SETs) and single-event functional interrupts (SEFIs). There are other types of SEE but this list comprises the major types of SEE.

An illustration of an ion strike is shown in Fig. 2.16. As the ion passes through the silicon lattice (or another semiconductor) it generates electron/hole pairs through direct and indirect ionization processes. Both drift and diffusion processes collect these excess carriers, but there is a temporal dependence as to whether drift or diffusion collection dominates. In short timescales post strike, drift collection dominates until enough charge has been removed for the p-n junction's space charge region (SCR) to reform. For longer time scales, diffusion processes dominate and electrons and holes diffuse across the SCR into the n-well and p-substrate respectively. Similar processes occur for ion strikes in vertical SiGe HBTs, except there are a total of three junctions in the active device volume (emitter-base and collector-base, and collector-substrate) that collapse and reform during an ion strike. The charge collected at the device terminals result in voltage and current transients (SETs), which may cause errors or failure in the parent circuit or system.

SEU and MBU occur in a digital circuit or system when an ion strike results in an unwanted bit flip (or multiple flips for MBU), corrupting a data stream. The digital system recovers once the radiation-induced transients subside. A SEFI is a soft error that causes a digital component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require a power cycle to restore operation. SEFIs usually occur when an ion strike corrupts a control bit or register. SEL, on the other hand, is an abnormal high-current state that causes a digital component to malfunction. If the device is not permanently damaged from SEL, power cycling is necessary to restore normal operation. An example of SEL for a CMOS device occurs when the passage of an energetic particle creates a parasitic bipolar (p-n-p-n) structure that effectively shorts the power rail to ground via a positive feedback loop. SEGR occurs when an ion strike on a MOSFET results in the breakdown of the gate dielectric,

which creates a conducting path through the gate oxide. SEGR causes an increase in gate leakage current and can result in device degradation or complete failure.

2.3 Summary

Ionizing radiation poses several threats to electronic systems in deep-space, interplanetary, and orbital spacecraft. Two important radiation effects for electronics are total ionizing dose (TID) and single-event effects (SEE). TID occurs when ionizing radiation generates electron/hole pairs that migrate and become trapped at oxide interfaces. The generation/recombination (G/R) traps created by these carriers can cause shifts in device performance (e.g., parasitic leakage paths, threshold voltage shifts, etc.) that can degrade the performance of the larger circuit or system. SEE, on the other hand, are operational disturbances within an electronic system caused by the passage of high-energy particles through a sensitive node. The system response to the aforementioned effects is highly dependent on the device, circuit, and system topology, therefore a semiconductor technology must be thoroughly characterized before it can be deemed suitable for radiation-intense environments.

CHAPTER 3

SILICON-GERMANIUM TRANSISTORS IN THE INVERSE-MODE OPERATING REGIME

3.1 Motivation

Comprehensive studies across multiple SiGe BiCMOS technologies have established that SiGe HBTs (and the circuits built from them) are highly tolerant to multi-Mrad TID exposures [80–87]. The enhanced TID immunity present in modern generations of SiGe HBTs (third-generation and up) is attributed to the "raised extrinsic base" structure of the bipolar transistor shown in Fig. 3.1, where the emitter-base and collector-base junctions are further removed from the shallow trench isolation (STI) oxide interface [80]. However, the vertical structure of the SiGe HBT and the presence of three sensitive junctions (emitter-base, collector-base, and collector-substrate) make it very effective at collecting radiation-induced charge carriers, the worst-case scenario being in high-speed digital circuits. SiGe bipolar logic without

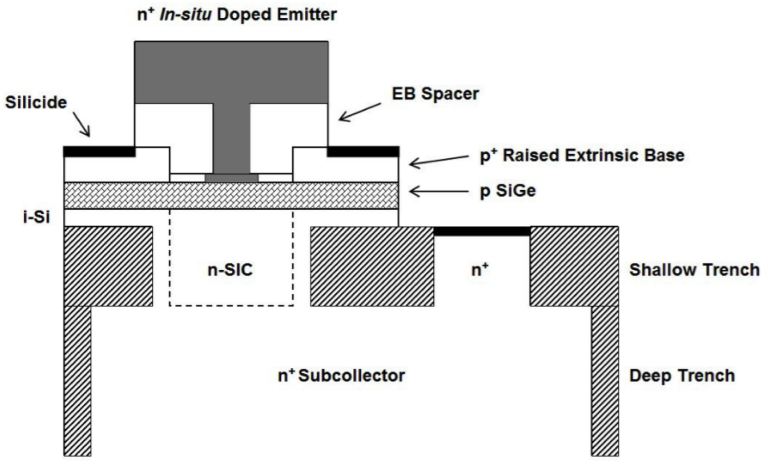


Figure 3.1: Schematic cross-section of a representative third-generation SiGe HBT with a "raised extrinsic base" architecture (after [79]).

device or circuit-level RHBD techniques have high saturated cross-sections and low SEU thresholds due to the prolonged charge collection mechanisms in the lightly-doped silicon substrate [88, 89].

Several circuit-level RHBD methodologies have been demonstrated to reduce the sensitivity of SiGe-based digital circuits, but these SEE mitigation techniques bear a penalty of increased circuit complexity, design footprint, and power consumption [90, 91]. Furthermore, as device-scaling and application constraints drive SiGe HBTs into picosecond operating regimes, which are on the same timescale as radiation-induced transient current pulses, circuits envisioned at advanced SiGe nodes will have to contend with these increasingly aggressive transient phenomena. Therefore, there is considerable interest in both understanding these effects at a fundamental level and then developing effective low-overhead, device-level RHBD techniques for mitigating the SEE response of SiGe devices and circuits [92–97].

While it has been demonstrated that single SiGe HBTs under inverse-mode operation (emitter and collector terminal exchanged) have potential for improving SEU sensitivity in high-speed digital circuits [2], that investigation was primarily focused on a first-generation SiGe-on-SOI platform, where a buried oxide layer physically isolated the collector-substrate junction, a sensitive region that can affect a circuit's overall SEU response. Inverse-mode SiGe HBT operation as a viable path on bulk SiGe platforms remains unexplored. The present investigation has two major goals: 1) to offer the first experimental heavy-ion data on SiGe Gbps shift registers for both forward and inverse-mode operation on a new fourth-generation bulk SiGe BiCMOS platform (IBM 9HP) and 2) to expand our current understanding regarding the use of inverse-mode operation for SEU mitigation in bulk SiGe technology platforms.

3.2 Inverse-Mode Operation of SiGe HBTs

Traditionally, SiGe HBTs within high-speed digital and RF circuits are designed to operate in "forward-mode," where the base-emitter (BE) and collector-base (CB) junctions are forward-biased and reverse-biased, respectively. This regime of operation provides maximum current gain, transconductance, and dynamic performance due to the asymmetrically doped emitter and collector regions and the presence of a Ge-induced electric field in the base which facilitates base minority carrier transport from the emitter to the collector. In the inverse-mode operating regime, the emitter and collector terminals are electrically swapped, so the physical collector now functions as the "electrical" emitter and the physical emitter functions as the "electrical" collector. Classically, the increased base width and device parasitics, coupled with the lower doping of the selectively-implanted collector (SIC) severely degrade the inverse-mode *dc* and *ac* performance, rendering that operational mode not useful, but it has been demonstrated that technology scaling (both in vertical and lateral dimension) will improve the inverse-mode performance of SiGe HBTs [98]. Furthermore, novel layout techniques can be employed to further optimize inverse-mode performance, leading to inverse-mode f_T that approach forward-mode f_T [99].

For the present discussion, the term emitter and collector will refer to the "electrical" definition, or in other words, the physical emitter and collector in forward-mode operation, or the physical collector and emitter in inverse-mode operation. The SiGe HBTs utilized for both forward-mode and inverse-mode shift registers have not been optimized in any way in order to better capture the innate performance of this current, state-of-the-art technology platform.

3.3 Heavy-Ion Broad-Beam Testing

To extend our understanding of inverse-mode operation and its use in a bulk SiGe platform, forward-mode and inverse-mode 16-bit digital serial shift registers utilizing

a standard master/slave architecture were designed using IBM's state-of-the-art 9HP SiGe BiCMOS process [13]. This fourth-generation bulk SiGe BiCMOS process offers 90 nm CMOS and *npn* SiGe HBTs with a peak f_T and f_{MAX} of 300 GHz and 350 GHz, respectively. Both forward-mode and inverse-mode shift registers incorporated an RHBD gated-feedback cell (GFC) clock tree, which utilized forward-mode and inverse-mode HBTs, respectively. The input and output buffer stages for both shift registers were designed using forward-mode SiGe HBTs to maximize the output voltage swing.

The shift registers were die-attached, wirebonded onto custom-designed high-frequency test packages, and taken to Lawrence Berkeley National Laboratory's BASE facility where they were irradiated with a 10 MeV/amu heavy-ion cocktail across multiple incidence angles. All test packages were monitored in-beam with an Anritsu MP1764 BERT analyzer, utilizing a 127-bit pseudo-random pattern generator and error detector. The biasing schemes for the forward-mode and inverse-mode shift registers were identical. While the forward-mode shift register was capable of up to 12.5 Gbps data rates (the maximum throughput of the Agilent BERT analyzer), all comparisons are done at 1.0 Gbps as well as 1.5 Gbps data rate, the maximum data rate of the inverse-mode shift register. It should be noted that this discussion is the first demonstration of $>$ 1.0 Gbps inverse-mode SiGe bipolar logic utilizing standard, unoptimized SiGe HBTs. A photograph of one of the irradiation chambers located at the LBNL BASE facility (Cave 4A) is shown in Fig. 3.2. These complex enclosures, commonly called caves, can accommodate a variety of electronic packages, mounting options, and radiation sources. For example, Cave 4B at the LBNL BASE facility is the dedicated experimental chamber for heavy-ion and low-energy proton beams from the 88-inch cyclotron [100].

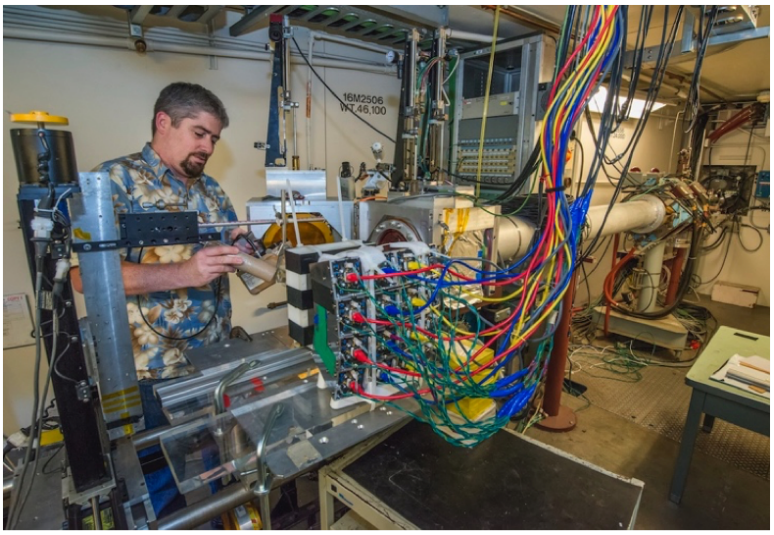


Figure 3.2: An example of one of the irradiation chambers located at the BASE facility at Lawrence Berkeley National Laboratory. This chamber is BASE Cave 4A which is reserved for high-energy proton irradiation with energies up to 55 MeV (after LBNL, courtesy of Michael Johnson).

The measured 1.5 Gbps bit-error cross-section curves for the forward-mode and inverse-mode SiGe shift registers at normal incidence as well as at fifteen and thirty degrees are plotted in Fig. 3.3 and Fig. 3.4, respectively. While the inverse-mode shift register displayed a reduced error cross-section for lower LET ion strikes, it exhibited as much as a 2× increase at higher LETs. This elevation in error cross-section conflicts with previous findings for inverse-mode shift registers designed in Texas Instruments' first-generation, complementary SiGe BiCMOS-on-SOI process (CBC-8), where a SOI inverse-mode shift register operating at a maximum data rate of 250 Mbps displayed an error cross-section improvement across all ion-strike LETs [2].

To offer a comparison and better understand the mechanisms driving the fundamental difference between the bulk and SOI hardware, the bit-error cross-section curves for both the forward and inverse-mode shift registers at 1 Gbps data rate are shown in Figs. 3.5 and 3.6. At this reduced data rate, the inverse-mode shift register exhibited a sharp reduction in bit-error cross-section across all heavy-ion LETs,

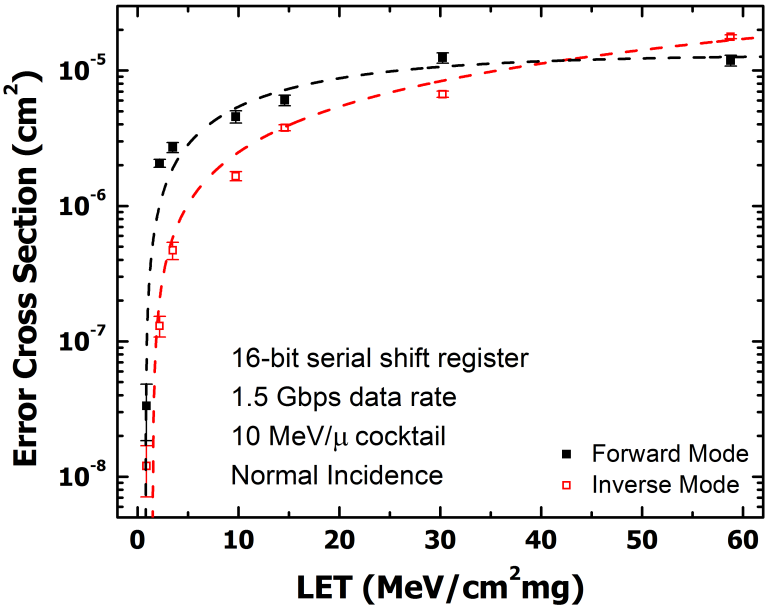


Figure 3.3: Measured bit-error cross-section curves for the 16-bit forward-mode and inverse-mode shift registers operating at 1.5 Gbps data rate as a function of LET at normal incidence.

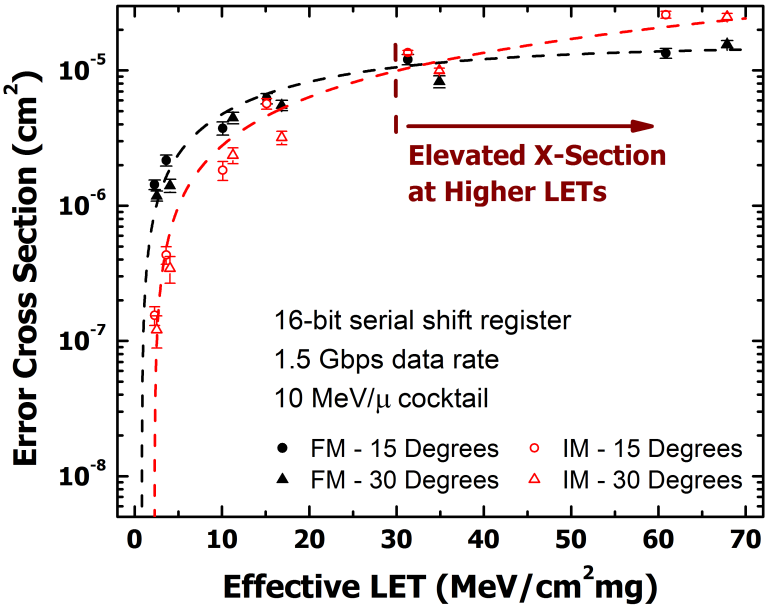


Figure 3.4: Measured bit-error cross-section curves for the 16-bit forward-mode and inverse-mode shift registers operating at 1.5 Gbps data rate as a function of LET at incidence angles of fifteen and thirty degrees.

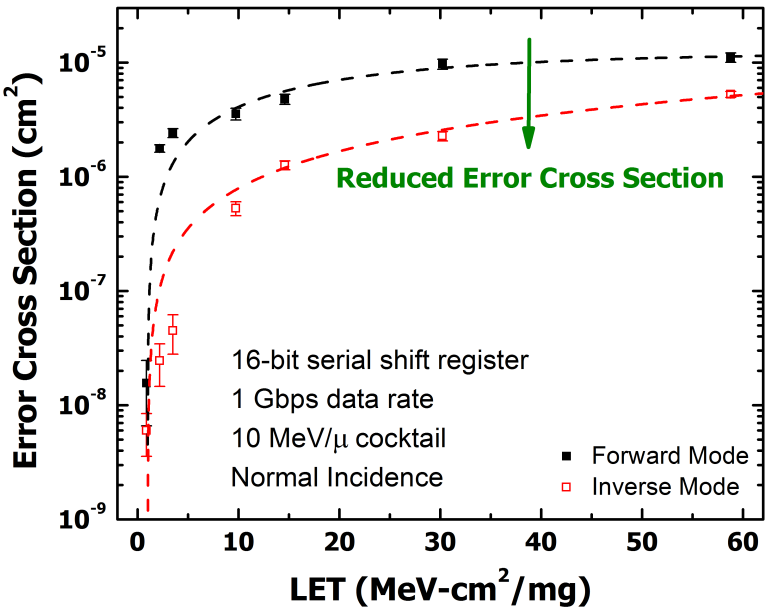


Figure 3.5: Measured bit-error cross-section curves for the 16-bit forward-mode and inverse-mode shift registers operating at 1 Gbps data rate as a function of LET at normal incidence.

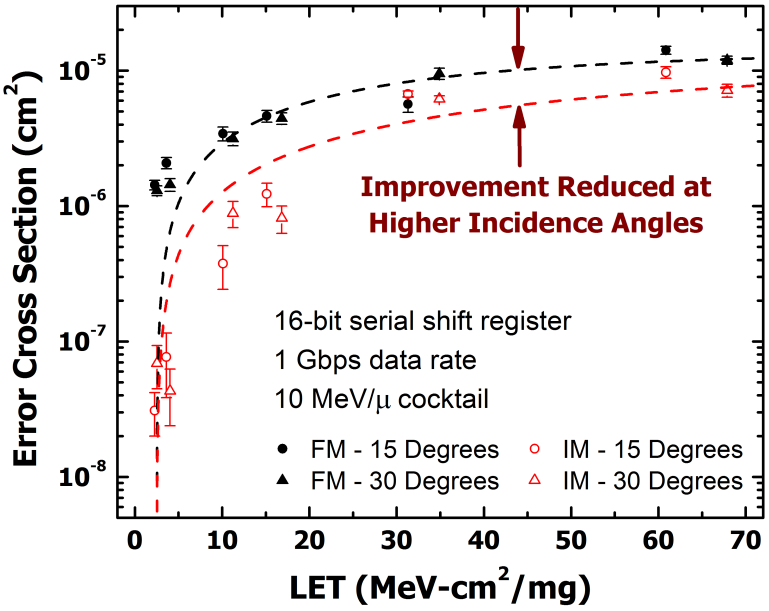


Figure 3.6: Measured bit-error cross-section curves for the 16-bit forward-mode and inverse-mode shift registers operating at 1 Gbps data rate as a function of LET at incidence angles of fifteen and thirty degrees.

with a reduction of approximately one order of magnitude for ion strikes with orbital-relevant LETs below 10 MeV-cm^2/mg. The error cross-section reduction achieved through inverse-mode operation in the fourth-generation shift registers was more pronounced when compared to previous first-generation hardware particularly at higher ion-strike LETs. This result is attributed to the aggressive doping profiles changes from SiGe BiCMOS technology scaling and will be discussed in more detail in the following discussion. The threshold LET for both shift registers remained the same at approximately 1 MeV-cm^2/mg.

The forward-mode shift register displayed greater sensitivity in its SEU response as the incident angle was increased, but the variability decreased for higher energy strikes. This dependence on incidence angle is attributed to the sensitive collector-substrate junction, a SEU-sensitive region that is only significant for bulk SiGe HBTs operating under forward-mode bias. For large incident angles, the probability of a heavy ion passing close enough to the collector-substrate junction of a sensitive node increases dramatically, leading to an elevation in the bit-error cross-section. Since the "electrical collector" (output) of a bulk inverse-mode SiGe HBT is physically decoupled from this junction, this observed dependence between bit-error cross-section and incidence angle is reduced. However, the improvement provided by inverse-mode operation diminishes at higher ion-strike LETs, which suggests that the high-LET heavy ions are depositing sufficient charge to influence both the emitter/base/collector stack (sensitive for both forward and inverse-mode HBTs) as well as the larger collector-substrate junction (sensitive only for forward-mode HBTs).

The previous four figures focused on bit-error cross-section, which is defined as the total number of bit errors divided by the total ion fluence. These cross-sections take into account single-event upsets (SEU), multiple bit upsets (MBU), and clock tree upsets. Due to the reduced dynamic performance of the inverse-mode SiGe HBT, the clock tree utilized in the inverse-mode shift register may be driving the increase in

error cross-section for high-LET ion strikes observed in Fig. 3.3 and Fig. 3.4. In order to decouple the clock tree upsets and MBUs from SEUs and estimate the impact of the forward-mode/inverse-mode clock trees on the total bit-error cross-section, the difference between bit errors and error intervals is shown in Fig. 3.7.

Error intervals, a dimensionless quantity calculated internally by the Anritsu BERT analyzer, increments if an error event occurs outside of a pre-defined time interval (1ms for this discussion). If multiple errors occur within this time interval, the BERT analyzer still registers the events as a single error interval; therefore a greater number of error intervals indicate that SEUs compose a majority of the total bit errors. In Fig. 3.7(a), the forward-mode shift register exhibits a minor increase in (bit errors – error intervals), which is expected since the faster clock rate has a greater probability of shifting multiple bits during a heavy-ion strike.

In Fig. 3.7(b), however, the inverse-mode shift register operating at 1.5 Gbps exhibits an abnormally large number of (bit errors – error intervals) at high ion-strike

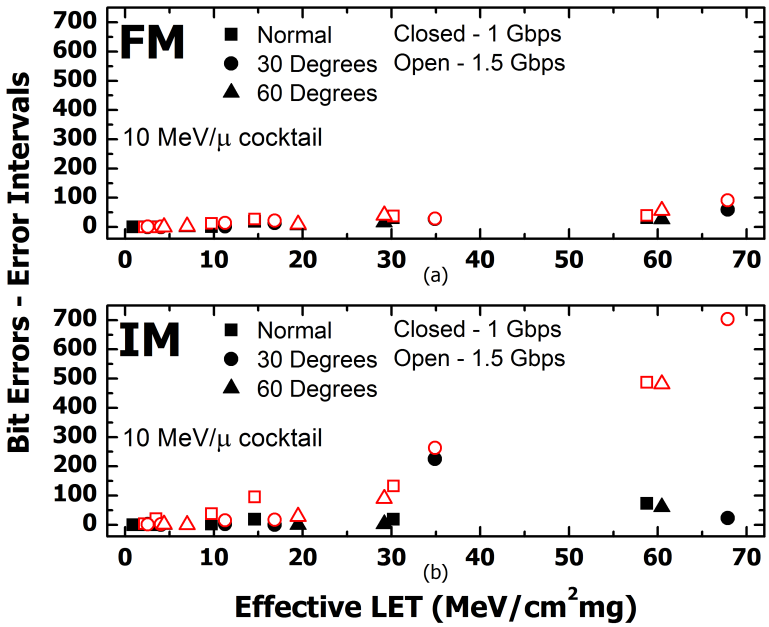


Figure 3.7: Difference in total bit errors and the number of bit error intervals measured by the Anritsu MP1764 BERT as a function of LET for (a) the forward-mode shift register and (b) the inverse-mode shift register at 1 Gbps and 1.5 Gbps data rates.

LETs. However, the inverse-mode shift register did exhibit similar MBUs and clock tree upsets as the forward-mode shift register at a data rate of 1 Gbps, which indicates that the inverse-mode clock trees functioned correctly at the reduced clock rate. The sharp increase in (bit errors – error intervals) at 1.5 Gbps, on the other hand, suggests that the inverse-mode clock trees were the primary driving factor for the increased bit-error rate in this region of operation. By comparing Fig. 3.7(b) with Fig. 3.3 and Fig. 3.4, it can be seen that the increase in clock tree upsets for the inverse-mode shift register at 1.5 Gbps coincides with the increased bit-error cross-sections observed for high ion-strike LETs. Therefore, the measured increase in error cross-section is an artifact of the internal inverse-mode clock tree in an unreliable operating regime. While the true peak operating speed of the inverse-mode shift register lies somewhere between 1 Gbps and 1.5 Gbps, it has been demonstrated that low-overhead layout techniques can improve the inverse-mode dynamic performance of a SiGe HBT [99]. Therefore, optimized fourth-generation SiGe HBTs should provide the capability of developing multi-Gbps, inverse-mode SiGe bipolar logic.

3.4 Pulsed-Laser Two-Photon Absorption (TPA) Testing

Laser-induced transients were measured at the Naval Research Laboratory (NRL) using carrier injection by through-wafer, two-photon absorption (TPA) via 150 fs, 1260 nm wavelength optical pulses, resulting in a 1 μm full width at half maximum (FWHM) focused spot size [101]. This system was employed because it enables 3-D, position-dependent, time-resolved measurements of single-event transients. Device test structures were packaged and wire bonded onto a custom-designed printed circuit board (PCB) that left the back substrate surface exposed for irradiation. Device biasing during irradiation was accomplished using Southwest Microwave SMA end launchers, low-loss SMA cabling, and Keithley 2400 source measure units. A photograph of the complete TPA SEE characterization system is shown in Fig. 3.8 while

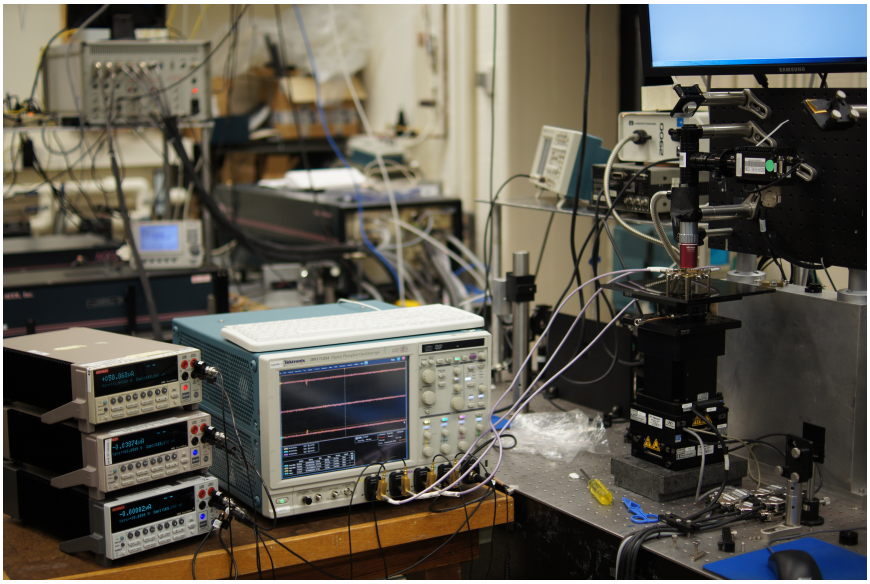


Figure 3.8: The TPA SEE characterization system at the Naval Research Laboratory, including Keithley 2400 source measure units and Tektronix DPO71254 real-time oscilloscope.

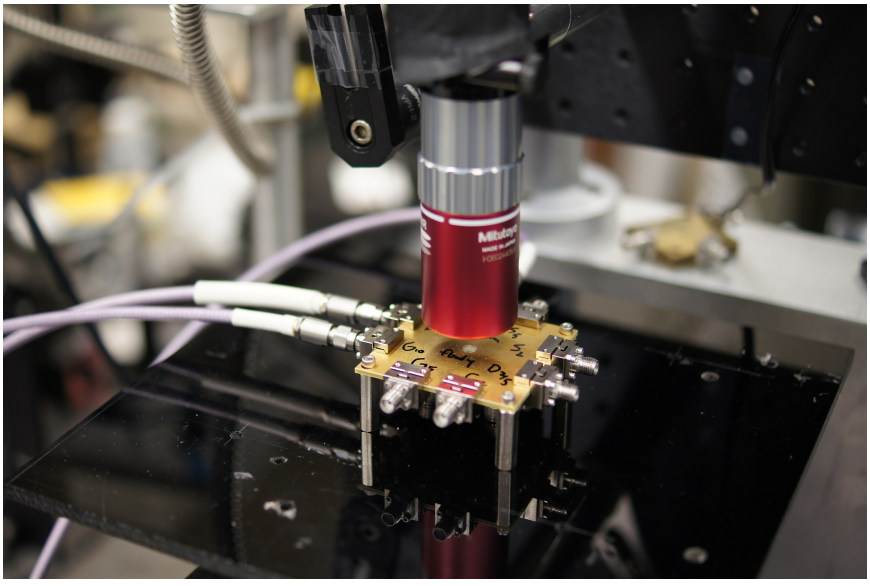


Figure 3.9: Custom high-frequency PCB packaging for heavy-ion SEE and TPA SET experimental testing. The board is mounted on the NRL TPA measurement station.

a zoomed-in view of the custom high-frequency PCB is shown in Fig. 3.9. The TPA system is capable of automated 3-D position and voltage sweeps, reducing interference from the end user and the measurement stage. In this approach, device-level current transients are induced via backside TPA. The resulting transients are then recorded using high-bandwidth measurement equipment, including a Tektronix DPO71254, 12.5 GHz, 50 GS/sec, real-time oscilloscope. The x-y-z translation platform has a position resolution of 0.1 μm and all 2-D raster measurements were collected with a step size of 0.25 μm, unless otherwise noted.

To support the heavy-ion SEU findings at the LBNL BASE 10 MeV/amu broad beam, 9HP SiGe HBT (0.1 μm $\times$ 2.0 μm) device test structures were characterized using through-wafer TPA SEE at NRL. In order to determine the differences in sensitive volume between forward-mode and inverse-mode 9HP SiGe HBTs, 2-D lateral scans were performed at fixed laser energy under a forward-mode (V_{CE} = 1 V) and inverse-mode (V_{EC} = 1 V) bias condition. The electrical collector transients (FM - physical collector, IM - physical emitter) under both biasing schemes are shown in Fig. 3.10 and Fig. 3.11 respectively. While the transient peak magnitude for both forward-mode and inverse-mode are similar, the SEE sensitive area (active area) under inverse-mode is dramatically reduced due to the electrical isolation between the bulk substrate and physical emitter terminal. The total sensitive area of the inverse-mode SiGe HBT is approximately 70% of the total sensitive area under forward-mode operation.

Similarly, the forward-mode and inverse-mode four terminal SiGe HBT output transients across laser energy are shown in Fig. 3.12 and Fig. 3.13, respectively. While the output transients under both biasing schemes increase monotonically with respect to higher laser pulse energies (PEs), the inverse-mode emitter transient at low PEs are substantially smaller (approximately 50%) than the equivalent forward-mode collector current transient across all ion energies, supporting the observed low-LET SEU

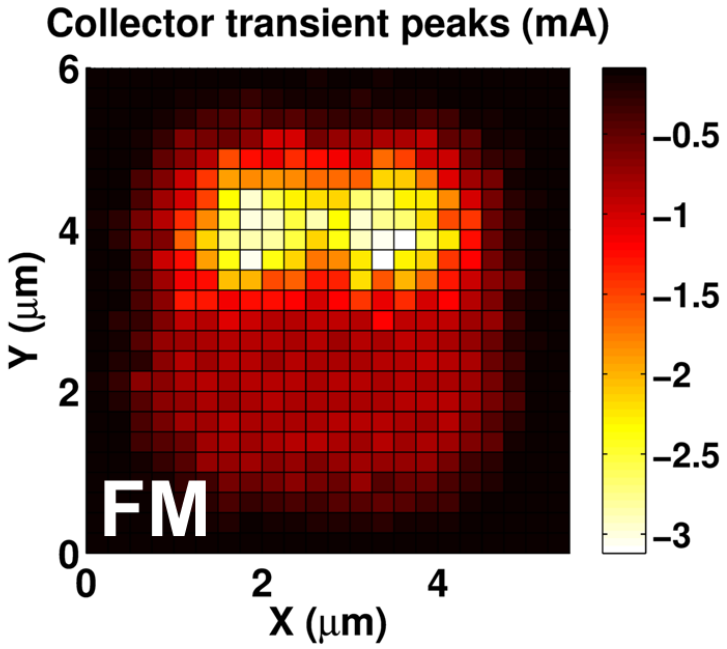


Figure 3.10: 2-D electrical collector (physical collector) output peaks for a 9HP (0.1 μm x 2 μm) SiGe HBT under forward-mode (V_{CE} = 1 V) bias. Laser energy = 1260 pJ.

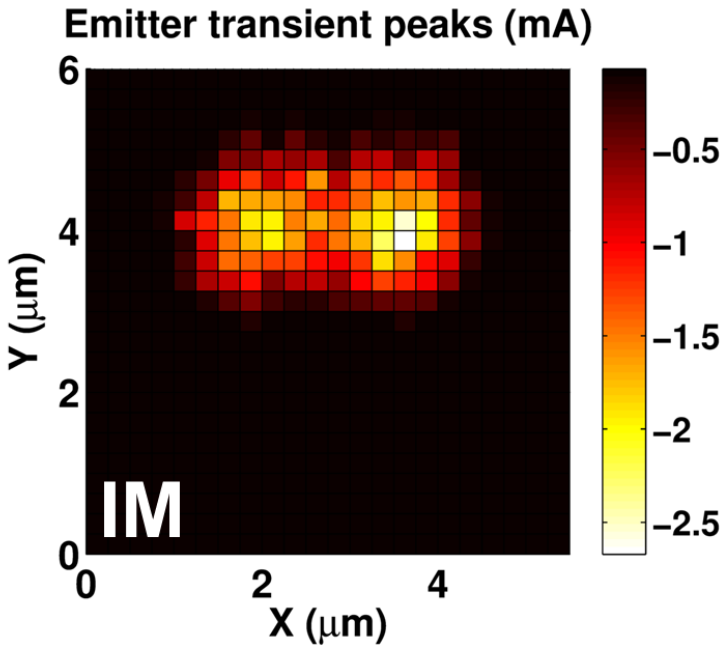


Figure 3.11: 2-D electrical collector (physical emitter) output peaks for a 9HP (0.1 μm x 2 μm) SiGe HBT under inverse-mode (V_{EC} = 1 V) bias. Laser energy = 1260 pJ.

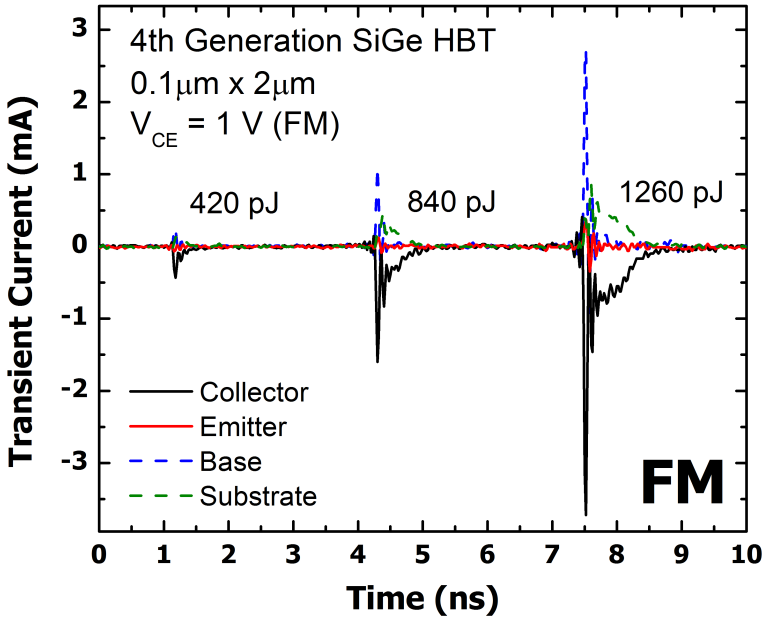


Figure 3.12: Measured current transients for a 9HP (0.1μm x 2μm) SiGe HBT under a forward-mode bias ($V_{CE} = 1$ V). Transients across multiple laser pulse energies (420, 840, and 1260 pJ) have been overlaid.

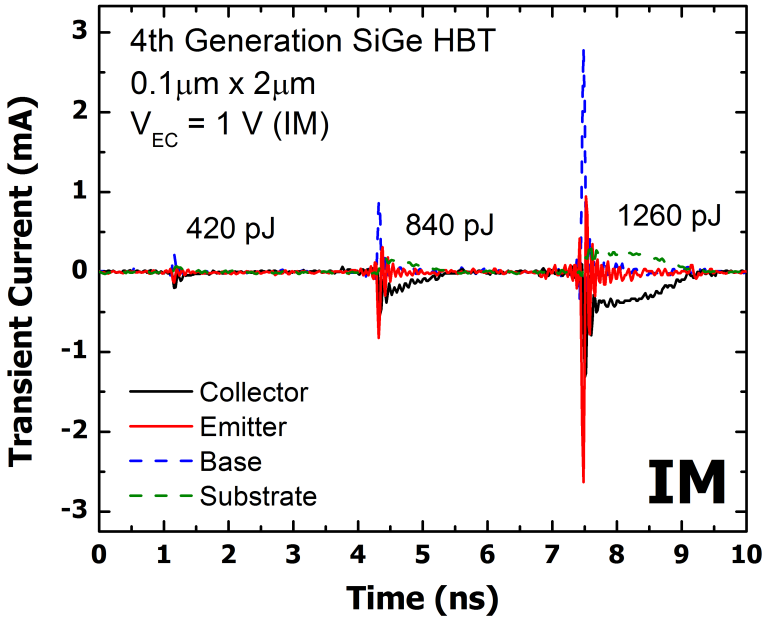


Figure 3.13: Measured current transients for a 9HP (0.1μm x 2μm) SiGe HBT under an inverse-mode bias ($V_{EC} = 1$ V). Transients across multiple laser pulse energies (420, 840, and 1260 pJ) have been overlaid.

improvement observed at heavy-ion broad beam. At higher PEs, the inverse-mode emitter transient and forward-mode collector transient peak magnitudes converge, but Fig. 3.14 shows that the inverse-mode emitter transient duration is significantly reduced. This is a welcome sign for ultra-high-speed digital circuits with clock frequencies on the order of ion-induced transient current signals.

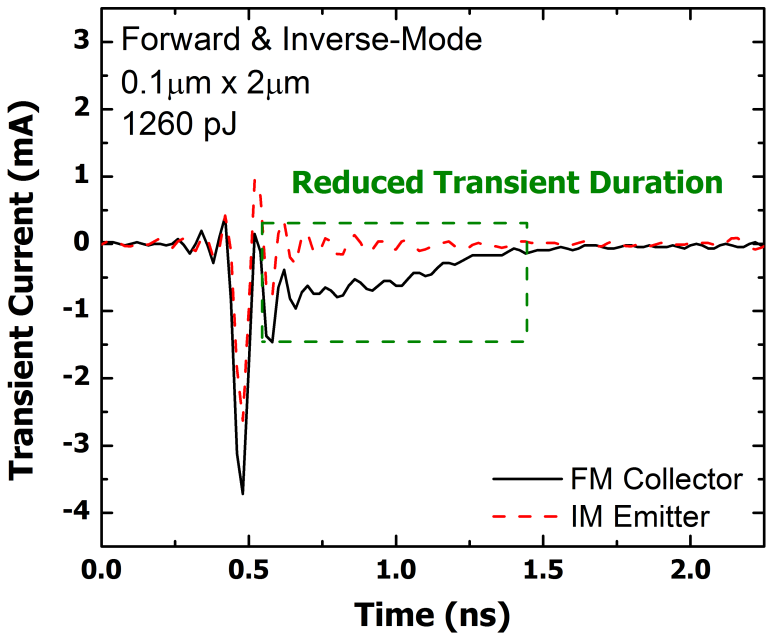


Figure 3.14: Measured forward-mode and inverse-mode electrical collector current transients for a 9HP (0.1 μm x 2 μm) SiGe HBT.

3.5 3-D TCAD Modeling and Simulations

3.5.1 Device-level TCAD Simulations

In order to fully understand the complex transient mechanisms occurring in these highly-scaled SiGe HBTs and provide a deeper understanding to the heavy-ion broad beam and pulsed-laser results, a 3-D model deck was developed for a 0.1 μm $\times$ 1 μm 9HP SiGe HBT within CFD Research Corporation's NanoTCAD software suite [102–105]. To ensure complete convergence for future fully-coupled mixed-mode simulations within Spectre, the TCAD model parameters were adjusted until the forward-mode performance closely matched that of the Spectre compact model. To provide

mixed-mode simulation capability for the inverse-mode shift registers, the Spectre compact model was modified to match the inverse-mode *dc* characteristics of the 3-D NanoTCAD 9HP HBT model deck. This adapted compact model was only utilized for subsequent inverse-mode mixed-mode simulations. The forward and inverse Gummel characteristics for the TCAD and Spectre models are shown in Fig. 3.15, indicating very good agreement between the compact and 3-D TCAD models.

All subsequent device transient simulations were performed using the SiGe HBT physical emitter-center as the ion-strike location, since this represents the worst-case scenario for SiGe digital logic because the heavy ion passes through all three sensitive device junctions (emitter-base, collector-base, and collector-substrate). Previous circuit-level simulations on Gbps SiGe logic have verified that transients in the collector terminal of the off-state current-mode logic (CML) device in the master storage or slave pass cell is the primary driving mechanism for SEU in these circuits [106]. A schematic of a D-flip-flop (DFF) utilizing forward-mode HBTs is shown in Fig. 3.16,

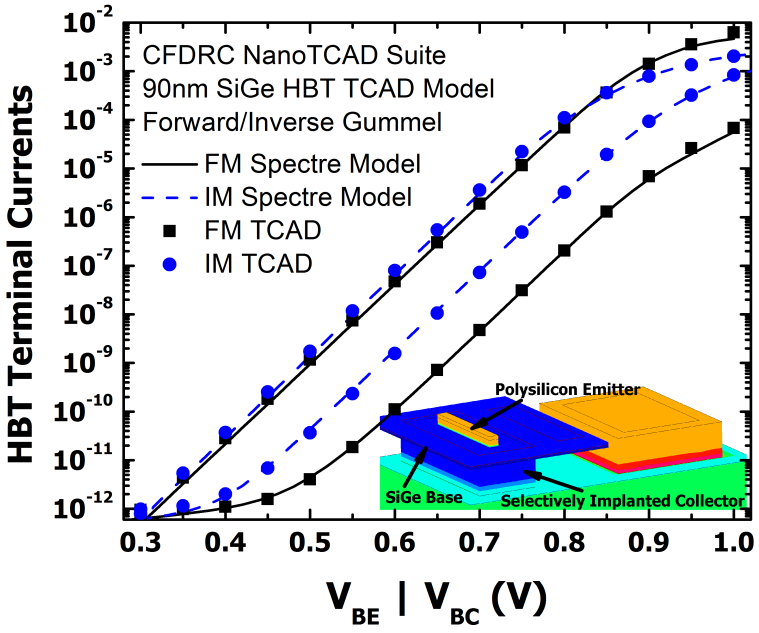


Figure 3.15: Forward and inverse Gummel simulations for both the Spectre 9HP compact model and *dc* calibrated 3-D NanoTCAD model. The compact model was modified to match the TCAD inverse-mode characteristics.

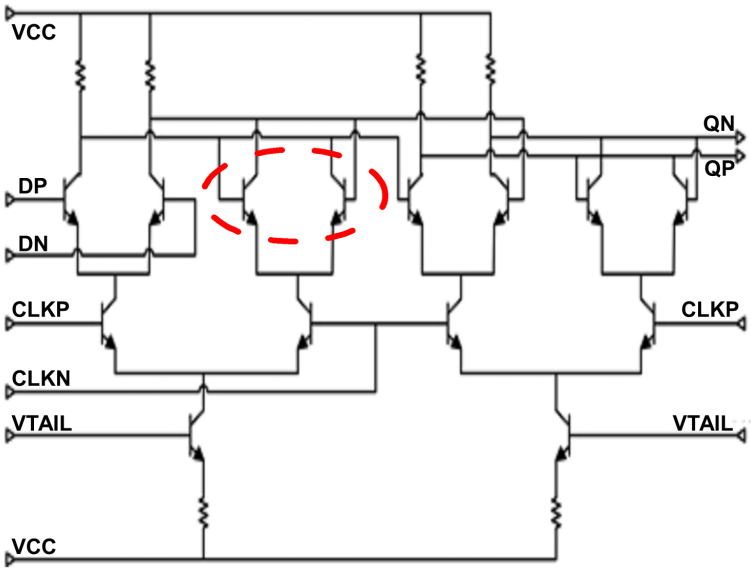
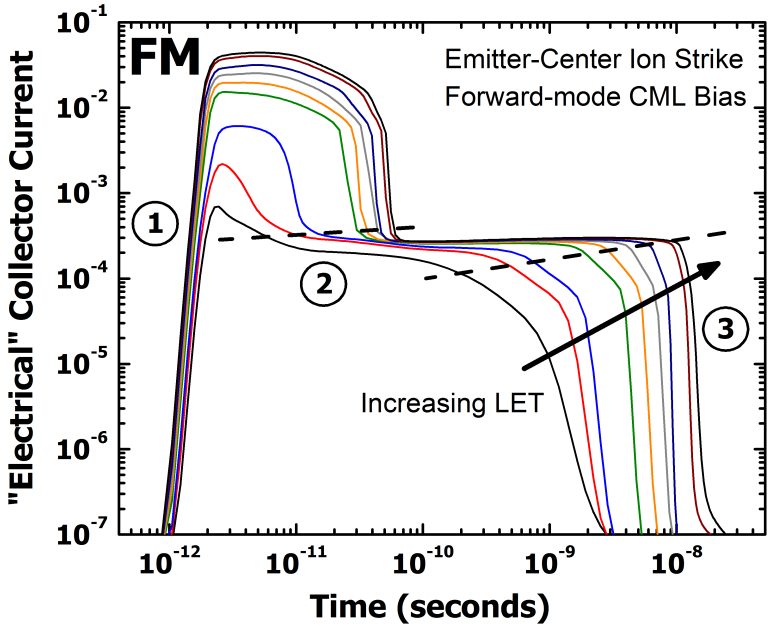


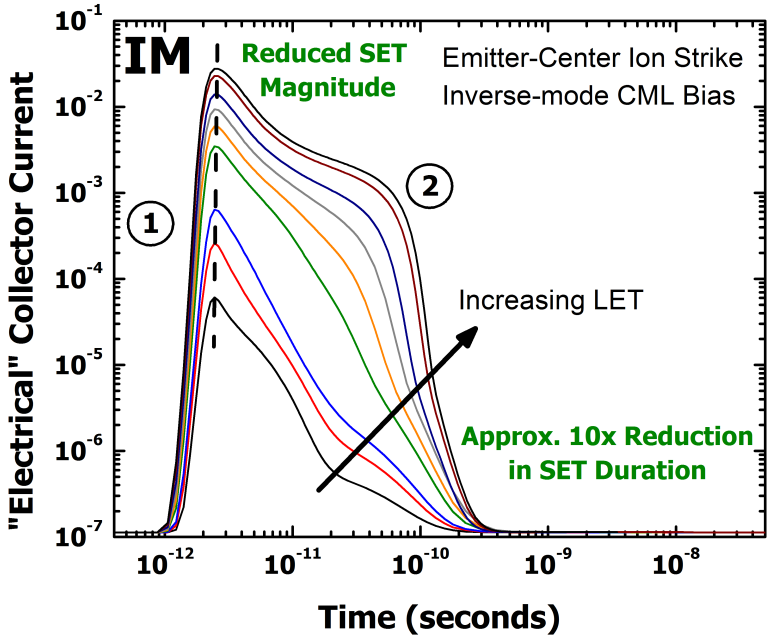
Figure 3.16: Circuit schematic of a forward-mode master/slave D flip-flop. The sensitive devices (master storage cell) have been highlighted.

highlighting the sensitive devices for the master storage cell. The 3-D TCAD model deck was biased to represent a forward-mode or inverse-mode CML off-state device (worst case). For a forward-mode device, this biasing scheme corresponds to a collector bias of 0 V, an emitter bias of -0.904 V, a base bias of -0.297 V and a substrate voltage of -3.3 V. The inverse-mode device has identical voltage biasing except the collector and emitter terminals are swapped. While these devices are biased on a negative rail (V_{CC} = 0 V, V_{EE} = -3.3 V), identical device biasing can be accomplished by shifting all voltage biases by 3.3 V, where V_{CC} = 3.3 V and V_{EE} = 0 V.

The simulated electrical collector transients for a forward-mode (physical collector) and inverse-mode (physical emitter) CML off-state device across multiple ion LETs are shown in Fig. 3.17. Unlike previous SiGe-on-SOI TCAD simulations, the forward-mode bulk collector transient can be delineated into three distinctive regions while the inverse-mode device exhibits the same two regions as explained at length in [2]. Region 1 arises from the collapse of the emitter-base and collector-base depletion regions from the large influx of charge carriers shortly after the ion strike. The high electric fields normally present in the collector-base depletion region push out



(a)



(b)

Figure 3.17: Simulated output current transients (electrical collector) for a 90 nm SiGe HBT operating in (a) forward-mode off-state bias (V_{CE} = 1 V) and (b) inverse-mode off-state bias (V_{EC} = 1 V) across multiple ion-strike LET (0.89 MeV-cm^2/mg to 58.78 MeV-cm^2/mg (10-MeV boron to 10-MeV xenon)).

across the narrow base to the emitter, resulting in a low impedance path for charge to flow between the collector and emitter terminals. This transient mechanism has been described in the literature as the "ion shunt" effect [107, 108]. The electric field lines driving the ion shunt will separate the ion-induced charge carriers (electrons and holes) in the vertical HBT stack until the charge carrier concentrations drop below the doping level on the lower-doped side of the depletion region (base). Once the ion-induced charge carrier concentrations have dropped below this critical level, the emitter-base and collector-base depletion regions reform, which eliminates the large drift component of the collector transient and marks the end of region 1.

Region 2 signals a departure of the similarities between the forward-mode and inverse-mode transient signatures. In region 2, the remaining ion-induced charge carriers present in the HBT stack are separated by the emitter-base and collector-base depletion regions. However, for the bulk forward-mode device, there is also a subcollector-substrate diffusion component that dominates shortly after region 1. In order to better differentiate the forward-mode and inverse-mode collector transient signatures, region 2 for the forward-mode device has been sub-divided into two distinct regions: 2 and 3.

In region 2, the excess charge carriers present in the p-substrate separate as electrons diffuse towards the subcollector-substrate depletion region, where they are swept up and collected at the physical collector terminal. The p-substrate for bulk SiGe processes is extremely thick compared to the emitter/base/collector HBT stack, so the charge concentrations present there can take a relatively long time to be collected at the collector terminal. This observation coupled with the fact that the subcollector-substrate depletion region can only sweep a finite number of charges per unit time results in the prolonged diffusion tail present in bulk SiGe collector transient waveforms. However, as the concentration of charge carriers in the p-substrate drops below the charge collection saturation threshold of the reverse-biased subcollector-substrate

junction, the collector transient current begins to decrease, marking an end to region 2. In region 3, any residual charges in the p-substrate and HBT stack are either collected by the emitter-base, collector-base, or subcollector-substrate depletion regions or are left to recombine, resulting in a very sharp decrease in collector transient current. Since the electrical collector (physical emitter) of the inverse-mode SiGe HBT is electrically isolated from the sensitive subcollector-substrate junction, the inverse-mode collector transient in Fig. 3.17(b) exhibits two important improvements in its collector transient signature, 1) a lower peak transient magnitude since the electrical collector current is no longer a superposition of the emitter-collector ion-shunt and substrate diffusion currents, and 2) an overall reduced transient duration. Both are important for SEU in high-speed logic.

While the absence of the subcollector-substrate diffusion tail is largely responsible for this reduction in total transient duration, the ion-shunt region (region 1) also exhibits a very large (approximately one order of magnitude) reduction in duration, similar to previous reports for SiGe-on-SOI inverse-mode HBTs [2]. To better understand the complex junction dynamics during the ion strike, the vertical electric field component of a 1-D "z" cut through emitter-center across multiple heavy ions for forward and inverse-mode biasing is shown in Fig. 3.18 and Fig. 3.19, respectively. In forward-mode operation the emitter-base and collector-base depletion regions collapse leading to the extended ion-shunt component seen in region 1 of Fig. 3.17(a).

From Fig. 3.19, the larger electric field present in the reverse-biased physical emitter-base (electrical collector-base) depletion region is not heavily affected by the presence of the ion-induced charge carriers. Since the physical emitter-base electric fields are not easily neutralized, elevated drift current levels can remove the excess ion-induced charges more quickly, resulting in the reduced ion-shunt duration seen for the inverse-mode device. Fig. 3.19 also demonstrates the impact of device scaling with respect to the inverse-mode SEE response. The residual electric fields in the physical

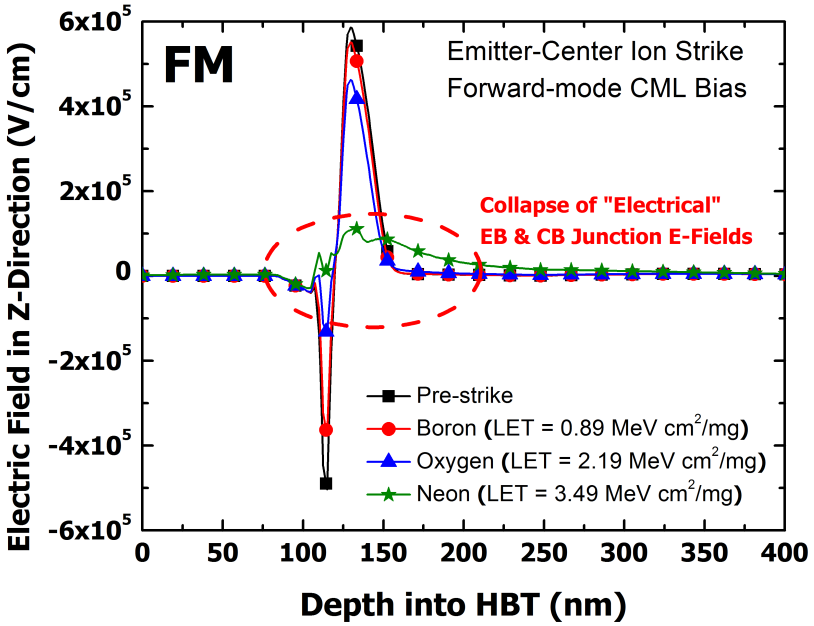


Figure 3.18: Simulated vertical electric field lines through the center of a bulk 90 nm SiGe HBT, biased in the forward-mode operating regime, before and directly an ion strike for a variety of different low-LET ions.

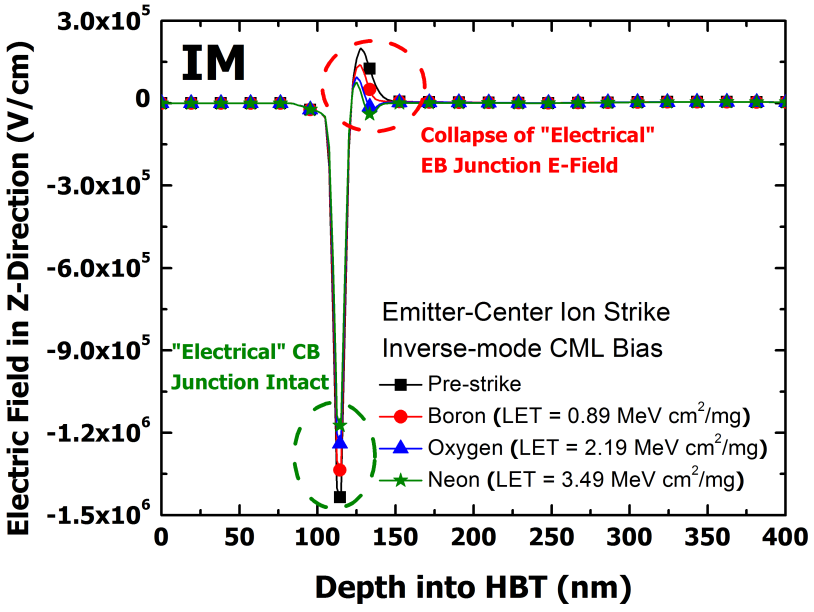


Figure 3.19: Simulated vertical electric field lines through the center of a bulk 90 nm SiGe HBT, biased in the inverse-mode operating regime, before and directly an ion strike for a variety of different low-LET ions.

emitter-base depletion region are much higher than the post-strike fields reported for first-generation SiGe BiCMOS devices (approximately -9×10^4 V/cm), indicating that as SiGe HBTs are laterally and vertically scaled, the associated aggressive doping levels will drive further improvements in inverse-mode device and circuit-level SEE, which is clearly good news. It should be noted, however, that reverse-biasing the emitter-base junction for these highly-scaled nodes will present potential reliability issues that need to be considered.

3.5.2 Circuit-Level Mixed-Mode Simulations

Mixed-mode TCAD modeling techniques utilize a fully-coupled approach where a single device within the circuit is replaced with a TCAD model deck [109, 110]. Since mixed-mode simulations couple external effects into the device-level transient waveform, these approaches should provide a more accurate representation of the overall circuit or system-level response. Previous work has shown that the circuit-level modeling approach (i.e., current-injection vs. mixed-mode) had a strong impact on simulation fidelity for high-speed, SiGe-based digital circuits [106]. However, it should be noted that the increased computational overhead and numerical convergence can become a significant problem, particularly for complex, multi-stage circuits and systems.

The following discussion provides an overview of the development process for a CFDRC mixed-mode (CFDRC MixCAD) circuit simulation. First, a circuit schematic is created within the Cadence Virtuoso design suite and transient simulations are utilized as a comparison point against laboratory measurements. The post-simulation operating point (circuit's final conditions) are saved to an external file and serve as the initial conditions for subsequent ion-strike TCAD simulations. In CFDRC NanoTCAD, the external device biases are altered to match the *dc* operating point of the test circuit and improve numerical convergence. Next, the Spectre netlist is saved

and the netlist parameters for a single device instance (FET, HBT, etc.) are removed. The relevant circuit nets for the DUT are redirected to the terminal contacts of the 3-D TCAD model, thereby allowing NanoTCAD to interface directly within the Spectre simulation environment. The direct coupling between NanoTCAD and Spectre makes this approach unique amongst other mixed-mode modeling techniques which may utilize simplified SPICE solvers and device models. By utilizing the complete and up-to-date PDK compact model, CFDRC MixCAD provides a close match to the original circuit specifications and previous studies have shown it to closely match experimental conclusions.

To expand our understanding of how inverse-mode operation affects circuit-level SEE, fully-coupled mixed-mode simulations were utilized to ascertain the SEU improvement of inverse-mode SiGe HBTs in high-speed digital logic. A CML off-state device in the master storage branch of a forward-mode and inverse-mode DFF was replaced with the 3-D TCAD model and subjected to a neon (LET = 3.49 MeV-cm^2/mg) emitter-center (worst case) ion-strike simulation. The DFF output voltage (QN) was monitored while the clock signal was pulsed to latch the transistor output (electrical collector) to the DFF output node. The delay of the clock edge transition to the ion strike was varied to determine the circuit-level SEU sensitivity to device transient duration. The output voltages for the forward-mode and inverse-mode DFF are plotted in Fig. 3.20. The forward-mode DFF exhibited SEU for clock transitions up to the simulated maximum delay of 0.8 ns. The inverse-mode DFF, however, did not exhibit SEU, even at post-strike clock delays as short as 0.1 ns. These results agree with previous TCAD simulations and show the potential of SiGe HBT inverse-mode operation as an effective SEE mitigation strategy.

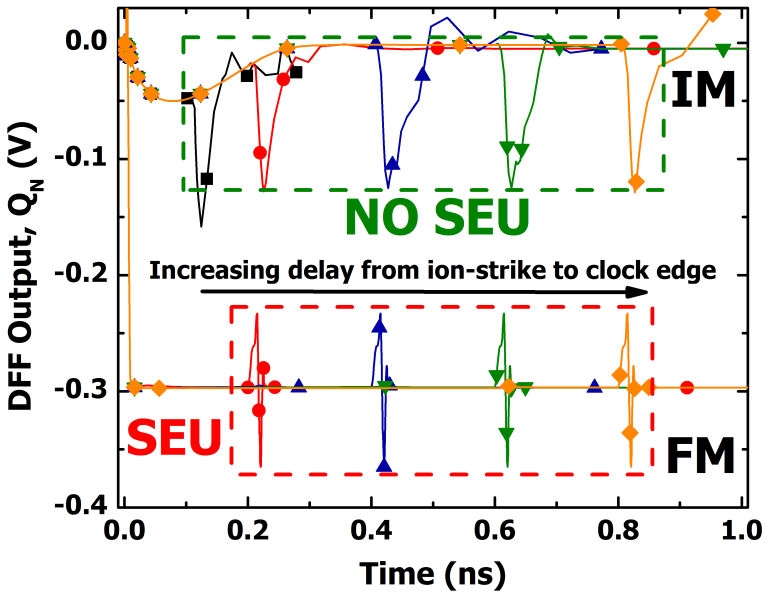


Figure 3.20: Mixed-mode voltage (QN) transients for a neon ion strike on the master storage CML-off device for forward-mode and inverse-mode DFF across multiple clock delays. The strike time was held constant at 2 ps.

3.6 Summary

Heavy-ion broad beam SEE results for a fourth-generation, 90 nm SiGe BiCMOS process show a large improvement in circuit-level SEU for circuits designed using inverse-mode SiGe HBTs. Since the mechanisms driving this improvement are a result of SiGe BiCMOS technology scaling, the inverse-mode performance and SEU mitigation potential are expected to increase as SiGe HBTs are driven towards smaller lithographic nodes. Furthermore, low-overhead optimization techniques can improve the dynamic performance of inverse-mode SiGe HBTs towards that of forward-mode devices. While standard master/slave shift registers were assessed in this discussion, the intersection of device-level, inverse-mode SEE mitigation techniques with established circuit-level SEU hardening approaches [90] may reveal strategies for developing multi-Gbps, SEE-tolerant SiGe digital logic.

CHAPTER 4

COMPLEMENTARY (*NPN* + *PNP*) SIGE BICMOS

4.1 Motivation

Traditionally, *npn* SiGe HBTs were the only SiGe device offered due to the reduced minority carrier mobilities of holes compared to electrons and the presence of a Ge-induced valence band offset, which can severely degrade the performance of SiGe *pnp* HBTs. However, careful modifications to BiCMOS process flows have allowed semiconductor foundries to incorporate the *pnp* HBT into modern SiGe BiCMOS technology to produce complementary SiGe BiCMOS (C-SiGe BiCMOS) platforms [16,111,112]. C-SiGe BiCMOS technology platforms commonly offer "matched" *npn* and *pnp* SiGe HBTs (matched-f_T), where the *pnp* design flow is optimized for peak dynamic (*ac*) performance and the matched *npn* SiGe HBT device profile is intentionally "slowed down" in order to provide similar *ac* characteristics. The availability of C-SiGe BiCMOS process design kits (PDKs) have helped push SiGe into a growing number of precision analog IC applications, including wireline telecommunication drivers, bipolar operational amplifiers, and DAC/ADCs [113]. While the exact proportion of *npn* and *pnp* HBTs vary across different circuit applications, high-performance *pnp* SiGe HBTs do allow designers to construct fully-bipolar circuits, which leverage the superior noise characteristics of SiGe HBTs for ultra-low-noise applications.

A previous SET study on a first-generation C-SiGe-on-SOI platform (CBC8) showed that *npn* and *pnp* SiGe HBTs exhibit similar sensitive areas to a 36-MeV oxygen microbeam [114]. However, the presence of a buried oxide layer and deep trench isolation (DTI) within this technology effectively isolates the collector/base/emitter

stack from the surrounding silicon substrate, making it difficult to assess the impact *pnp* HBTs may have on SET magnitude and duration, especially in regards to the extended charge sharing between the collector and bulk substrate regions. Additionally, the effects of SiGe BiCMOS technology scaling on the SET response of *pnp* SiGe HBTs have not been explored. The present investigation has three major goals: 1) to offer the first experimental SET data on a third-generation bulk C-SiGe BiCMOS platform (IHP SG25H3P), 2) to provide an understanding on the intrinsic transient mechanisms within bulk *pnp* SiGe HBTs, and 3) to ascertain the potential *pnp* SiGe HBTs may have as a SEE mitigation path for complementary analog and RF circuit blocks.

4.2 IHP SG25H3P C-SiGe BiCMOS

In order to characterize the transient behavior of modern, bulk *pnp* SiGe HBTs and provide a comparison with traditional bulk *npn* devices, single device test structures from the Institute of High Performance (IHP) Microelectronics third-generation SG25H3P platform were selected for SEE analysis. In addition to 0.25 μm CMOS, IHP SG25H3P provides a *pnp* SiGe HBT with a peak f_T and f_{MAX} of 90 GHz and 120 GHz, respectively [16, 115]. Previous studies on voltage controlled oscillators (VCOs) developed within this technology have shown that *pnp*-only designs yielded superior phase noise performance even though the devices themselves have a higher noise figure [116].

Schematic cross-sections detailing the matched *npn* and *pnp* SiGe HBTs are shown in Fig. 4.1. This process utilizes an ion-implanted subcollector that is laterally confined by the shallow trench isolation (STI). This novel collector structure which does not include a STI region between the collector and emitter contact regions, allows for precise control of the collector-substrate (C-Sub) and collector-base (CB) junction

areas, minimizing the associated device parasitics (e.g., collector-substrate capacitance (C_{CS}), base-collector capacitance (C_{BC}), and collector resistance (R_C)), thereby overcoming the limitations associated with epitaxial subcollectors commonly found in other SiGe BiCMOS processes [117]. The absence of deep trench isolation helps minimize the thermal resistance of the device, improving heat dissipation under elevated current densities near peak-f_T.

A table of relevant device parameters for both devices are listed in Table 4.1. In addition to these matched devices, a high-performance (*npn*-only) SiGe HBT with a peak f_T of 200 GHz is available for circuit applications that necessitate increased high-frequency performance. The device area of the *pnp* HBT was scaled to provide matched *dc* characteristics, resulting in the following device geometries: 0.21 μm $\times$ 0.84 μm for the *npn* SiGe HBT and 0.42 μm $\times$ 0.84 μm for the *pnp* SiGe HBT. While a previous study investigating the TID response of SG25H3P demonstrated that the *pnp* SiGe HBTs exhibit a distinct TID improvement, the SEE response of this complementary platform remains unexplored [118]. It should also be reiterated that IHP SG25H3P does not include deep trench isolation, effectively decoupling advanced isolation techniques from the C-SiGe HBT transient response.

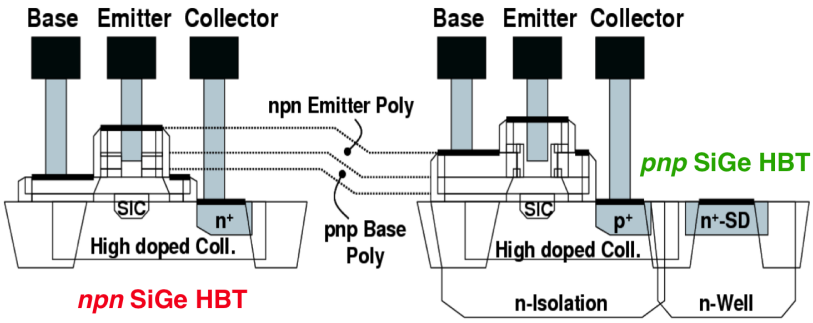


Figure 4.1: Schematic cross-sections of the IHP SG25H3P *npn* and *pnp* SiGe HBT (after [115]).

Table 4.1: Device parameters of matched *npn* and *pnp* SiGe HBTs from IHP SG25H3P SiGe BiCMOS (after [115]).

Parameter	Units	*npn*	*pnp*
β @ V_{BE} = 0.7 V		200	100
Peak f_T	GHz	110	90
Peak f_{MAX}	GHz	180	120
BV_{CEO} @ 10 μA	V	3.5	3.3
Minimum NF @ 5 GHz	dB	0.5	1.2

4.3 Pulsed-Laser TPA Testing

Laser-induced transients on single IHP SiGe HBTs were measured at the Naval Research Laboratory using the through-wafer, two-photon absorption (TPA) characterization system explained in detail in Section 3.4. All 2-D raster data were collected with a step size of 0.25 μm unless otherwise noted. The 2-D raster scans displaying the collector transient peaks for the *npn* and *pnp* SiGe HBTs in a forward-active (FA) bias (i.e., emitter-base junction forward-biased, collector-base junction reverse-biased), are shown in Fig. 4.2 and Fig. 4.3, respectively. The devices were biased to provide a steady-state collector current near peak-f_T, a relevant bias commonly encountered in high-performance RF amplifiers and high-speed bipolar logic applications. Comparing both figures reveals that the *npn* SiGe HBT exhibits an extended sensitive area due to charge carrier diffusion between the subcollector and substrate and the absence of DTI from the surrounding silicon substrate.

The *pnp* SiGe HBT in Fig. 4.3 displays two important improvements in its SET response; a lower SET magnitude across the entire device, as well as a substantial reduction (approximately 72%) in its sensitive area, where the sensitive area is defined as the region where the collector transient peaks ($|I_{C,peak}|$) are $\geq$ 0.50 mA. In addition to the 2-D collector transient peak plots in Fig. 4.2 and Fig. 4.3, the total collected charge at the collector terminal, an important indicator of SEE sensitivity,

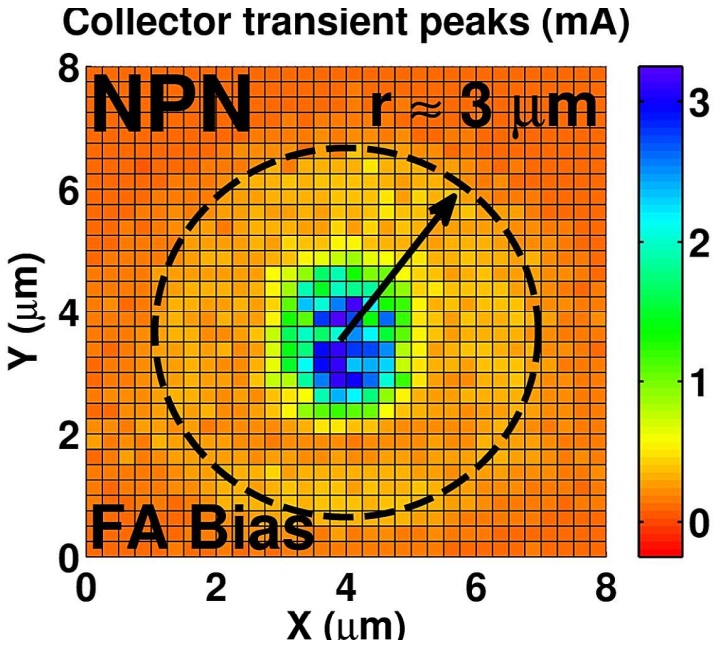


Figure 4.2: Measured 2-D collector output peaks for the *npn* SiGe HBT under a forward-active bias ($|I_C| \approx 1.113$ mA). The dashed ring represents the area of the device with a ($|I_{C,peak}|$) ≥ 0.50 mA.

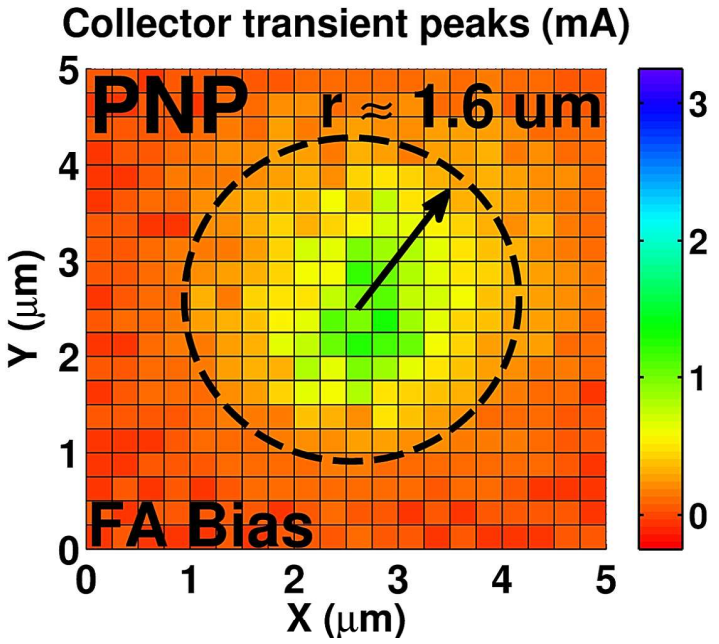


Figure 4.3: Measured 2-D collector output peaks for the *pnp* SiGe HBT under a forward-active bias ($|I_C| \approx 1.113$ mA). The dashed ring represents the area of the device with a ($|I_{C,peak}|$) ≥ 0.50 mA.

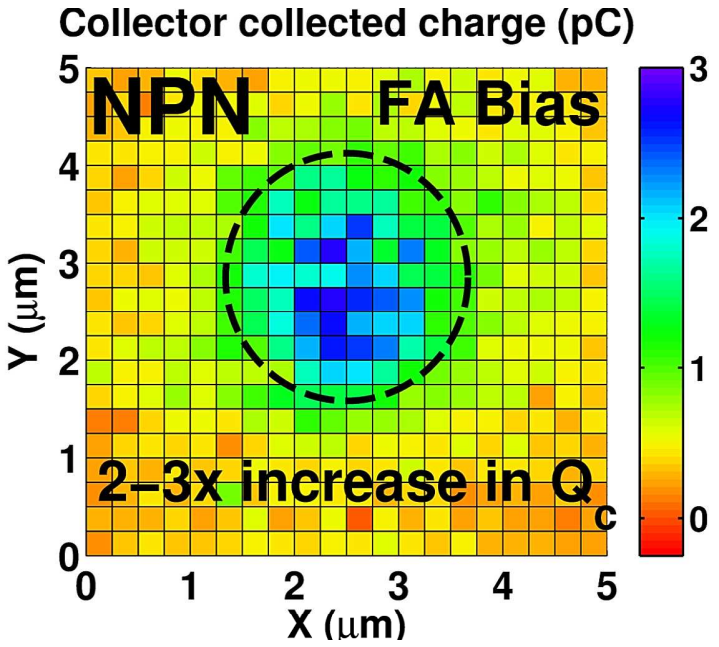


Figure 4.4: Measured 2-D collected charge at the collector terminal for the *npn* SiGe HBT under a forward-active bias ($|I_C| \approx 1.113$ mA). The dashed ring encompasses the vertical HBT material stack.

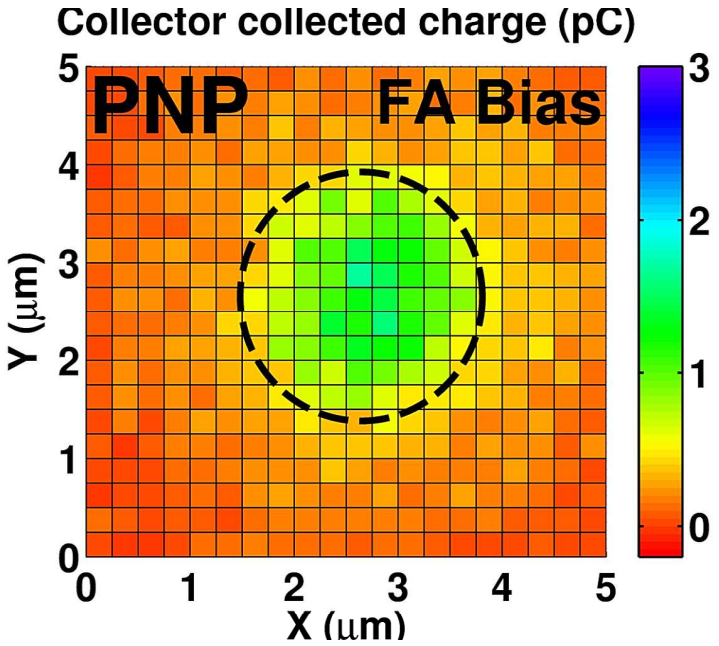


Figure 4.5: Measured 2-D collected charge at the collector terminal for the *pnp* SiGe HBT under a forward-active bias ($|I_C| \approx 1.113$ mA). The dashed ring encompasses the vertical HBT material stack.

for the *npn* and *pnp* HBTs under the FA bias are shown in Fig. 4.4 and Fig. 4.5, respectively. The dashed rings in these two figures encompass the vertical material stack (i.e., emitter/base/collector), representing the most SET-sensitive region of the SiGe HBT. Within this area, the *pnp* SiGe HBT exhibited up to a 3× reduction in charge collection. The significant improvements in sensitive area, transient peaks, and collected charge have important implications at the circuit and system level and suggest that circuits incorporating *pnp* SiGe HBTs will benefit from an improved SEE response.

To provide another bias point for comparison, the *npn* and *pnp* SiGe HBTs were irradiated under a forward-mode, off-state bias (V_C = 1 V, $V_B = V_E = V_{SUB}$ = 0 V for the *npn* HBT, V_C = -1 V, $V_B = V_E = V_{NW}$ = 0 V for the *pnp* HBT). This bias condition is commonly encountered within bipolar current-mode logic (CML) D-flip-flops (DFFs) and shift registers and previous studies have shown that the off-state bias is the most sensitive region of operation within these digital circuits [119–

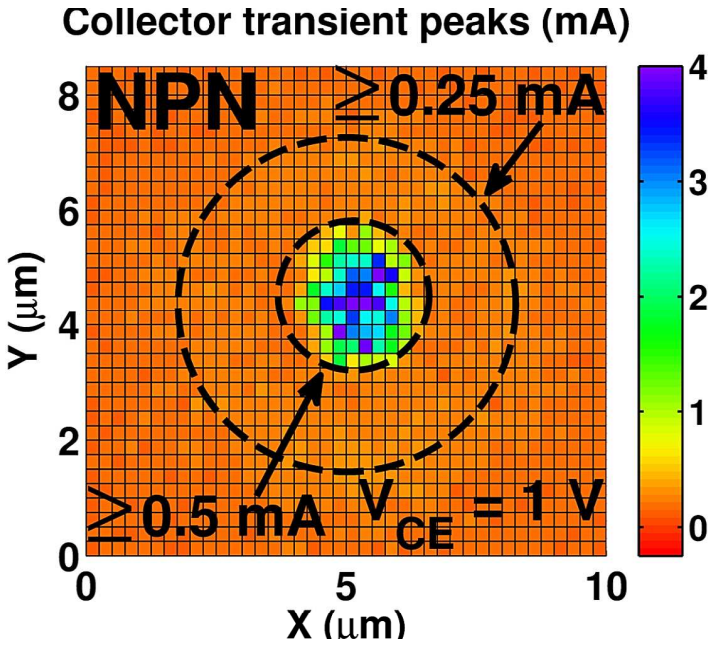


Figure 4.6: Measured 2-D collector output peaks for the *npn* SiGe HBT under a forward-mode, off-state bias (V_{CE} = 1 V, $V_{BE} = V_{SUB}$ = 0 V). Areas corresponding to $|I_{C,peak}| \geq$ 0.25 mA and $\geq$ 0.50 mA have been highlighted.

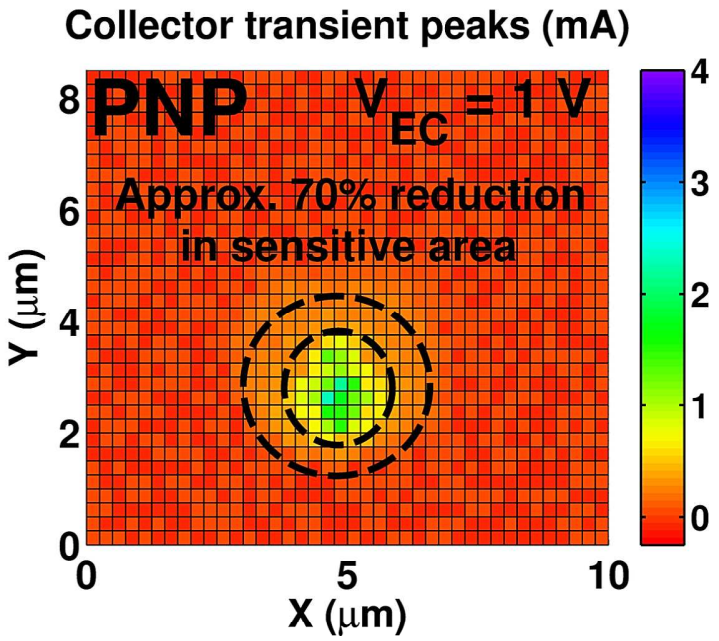


Figure 4.7: Measured 2-D collector output peaks for the *pnp* SiGe HBT under a forward-mode, off-state bias (V_{CE} = -1 V, V_{BE} = V_{NW} = 0 V). Areas corresponding to $|I_{C,peak}| \geq$ 0.25 mA and $\geq$ 0.50 mA have been highlighted.

121]. 2-D plots of the peak collector transient magnitude for both devices under a forward-mode, off-state bias, are shown in Fig. 4.6 and Fig. 4.7. Two rings have been superimposed on each figure, highlighting the areas where the collector transient peaks ($|I_{C,peak}|$) are $\geq$ 0.25 mA and $\geq$ 0.50 mA. Similar to the FA bias, the *pnp* SiGe HBT displayed a reduction in sensitive area by approximately 70%. The significant SET sensitivity improvements provided by the *pnp* SiGe HBT are interesting, given that its effective device area is twice that of the *npn* HBT, hinting that the differences of the electron/hole mobilities and lifetimes, as well as the presence of a moderately-doped n-well isolation layer may be responsible for the differences in laser-induced current transients.

While the previous 2-D investigations have suggested that the *pnp* SiGe HBT's SET improvement is inherently tied to effective isolation provided by the n-doped well, it is pertinent to analyze the time-domain properties of the *npn* and *pnp* transient response. In order to better understand these temporal characteristics and assess

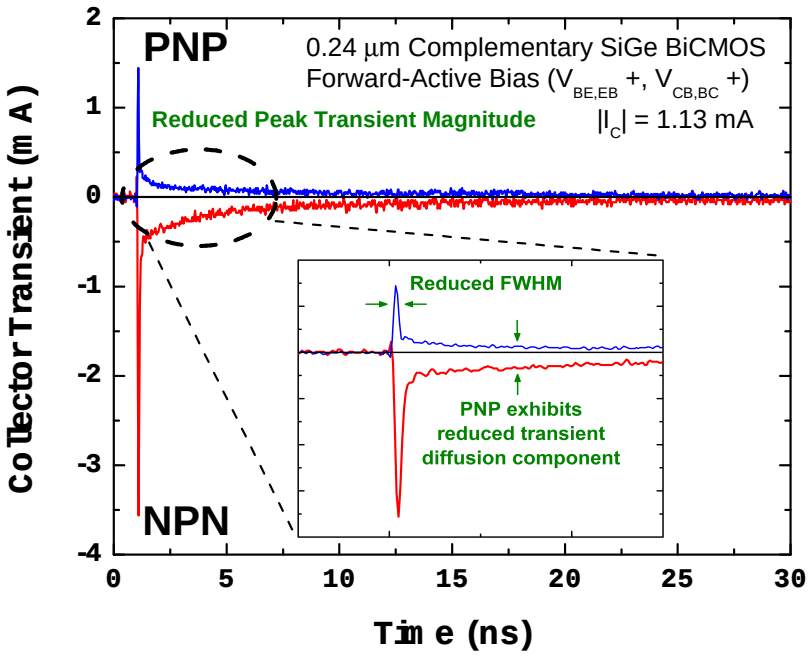


Figure 4.8: Measured collector current transients for the *npn* and *pnp* SiGe HBT under a forward-active bias ($|I_C| \approx 1.113$ mA).

the possible improvements *pnp* SiGe HBTs may provide with respect to transient duration, single transient waveforms at device-center (emitter-center) for both devices under a forward active bias ($|I_C| \approx 1.113$ mA) and a forward-mode, off-state bias ($V_{CE} = 1$ V, $V_{BE} = 0$ V, $V_{SUB} = 0$ V for the *npn* HBT and $V_{CE} = -1$ V, $V_{BE} = 0$ V, $V_{NW} = 0$ V for the *pnp* HBT) are shown in Fig. 4.8 and Fig. 4.9, respectively.

From Fig. 4.8, the *pnp* HBT shows three important improvements in its transient response: a reduced peak transient magnitude (agreeing with the previous 2-D raster scans), a faster transient spike (i.e., reduced full-width at half maximum (FWHM)), as well as a reduced transient diffusion component. The large transient spike is attributed to the "ion shunt" effect [107, 108], which leads to a large drift component induced by the electrical breakdown of the emitter-base, collector-base, and collector n-well (or collector-substrate) junctions within the SiGe HBT [1]. Therefore, the

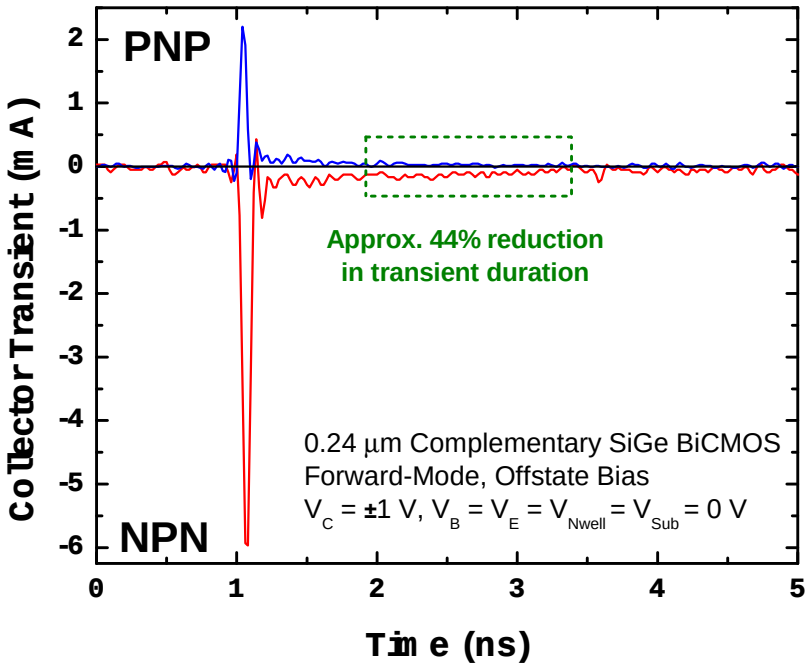


Figure 4.9: Measured collector transients for the *npn* and *pnp* SiGe HBT under a forward-mode, off-state bias ($V_{CE} = \pm 1$ V, $V_{BE} = V_{NW} = V_{SUB} = 0$ V).

reduction in FWHM suggests that the deposited charge within the *pnp* HBT is being collected more rapidly, leading to a faster re-establishment of the HBT depletion regions. The reduced transient diffusion component supports previous observations that the moderately-doped n-well effectively isolates the output terminal (collector) from the large charge carrier densities in the bulk substrate. As the n-well volume is significantly thinner than the underlying substrate, its drift and diffusion contribution on the collector terminal transient should be smaller than the equivalent substrate contribution for the *npn* HBT. This observation is evidenced in Fig. 4.9, where the *pnp* HBT exhibited a 44% improvement in transient duration. These experimental observations substantiate our previous claims that the differences in carrier mobilities/lifetimes as well as the possible isolation provided by the n-well layer may be driving the observed SET improvements.

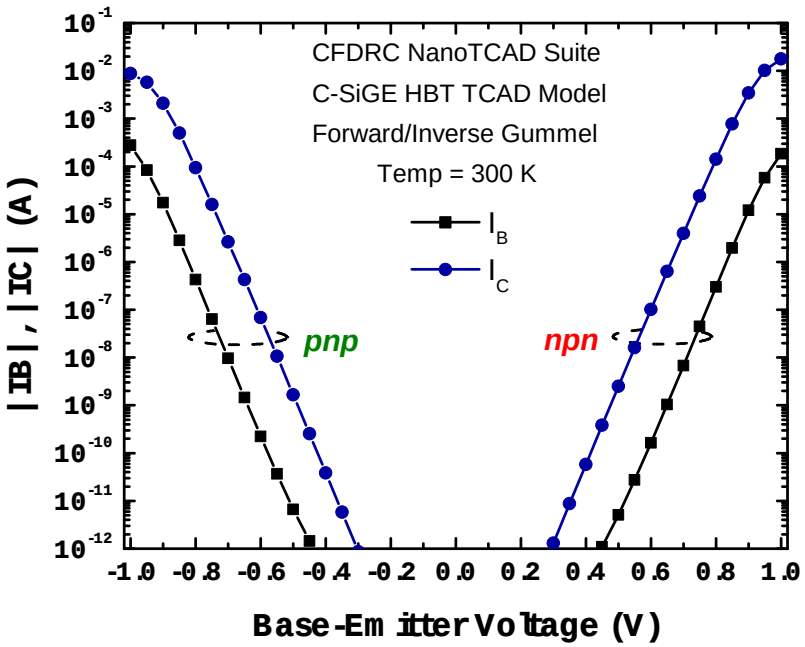


Figure 4.10: Forward Gummel simulations for the *npn* and *pnp* 3-D NanoTCAD models.

4.4 3-D TCAD Modeling and Simulations

To provide a deeper understanding of the physical phenomena responsible for the observed improvements during pulsed-laser TPA testing, 3-D TCAD model decks for both a *npn* and *pnp* SiGe HBT were developed using CFD Research Corporation's nanoTCAD software suite [102–105]. Identical emitter, base, and collector doping profiles were used for both models in order to simplify subsequent analyses and isolate the effects of the n-well isolation layer with respect to the collector transient response. The transfer characteristics (forward Gummel) for the *npn* and *pnp* TCAD models are shown in Fig. 4.10. All ion-strike simulations are assumed to be normal to emitter-center unless stated otherwise. The ion track depth was set to 11 μm to ensure sufficient charge deposition throughout all sensitive volumes.

Heavy-ion transient simulations across three different linear energy transfer coefficients (LET = 0.1, 1, and 10 MeV-cm^2/mg) were performed for both models under a forward-mode, off-state bias with the p-substrate and n-well doping densities at

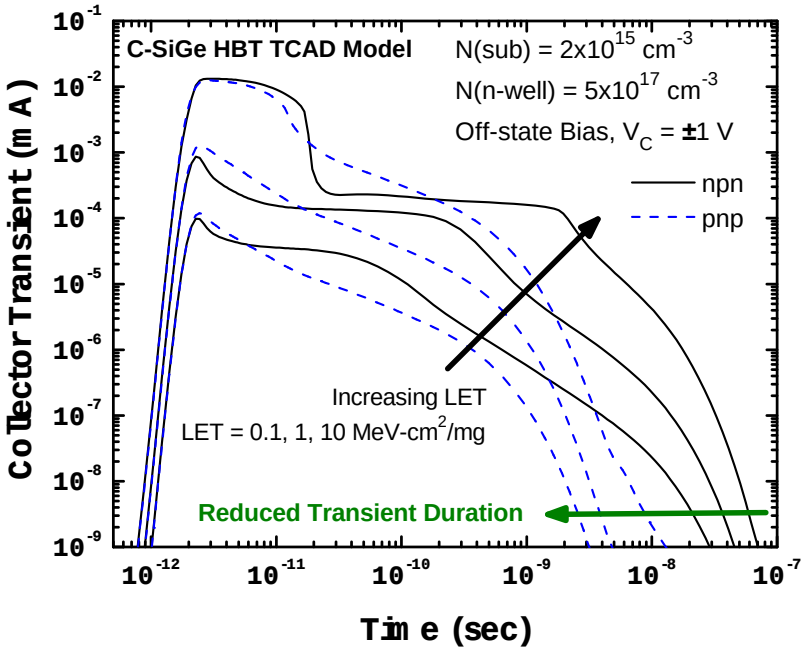


Figure 4.11: Simulated LOG_{10} collector current transients vs. LOG_{10} time for the *npn* and *pnp* 3-D NanoTCAD models under a forward-mode, off-state bias ($V_{CE} = \pm 1$ V, $V_{BE} = V_{NW} = V_{SUB} = 0$ V).

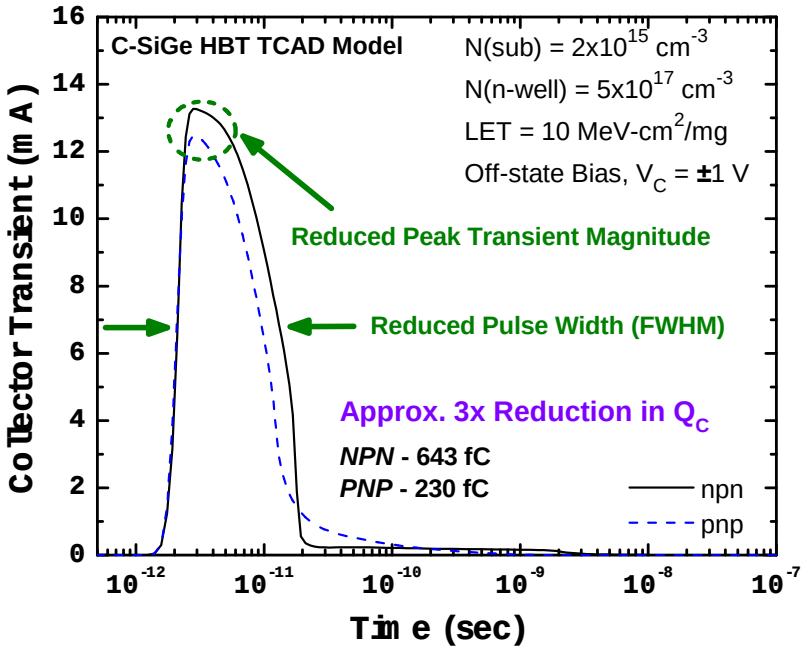


Figure 4.12: Simulated LINEAR collector current transients vs. LOG_{10} time for the *npn* and *pnp* 3-D NanoTCAD models under a forward-mode, off-state bias ($V_{CE} = \pm 1$ V, $V_{BE} = V_{NW} = V_{SUB} = 0$ V).

2×10^{15} cm^{-3} and 5×10^{17} cm^{-3}, respectively. The collector transient waveforms for the *npn* and *pnp* TCAD models are overlaid in Fig. 4.11. While the simulated *pnp* SiGe HBT exhibited a slightly larger peak transient magnitude at lower LET ion-strikes, the transient duration was reduced by as much as one order of magnitude across all ion-strike LETs. In order to better visualize the current transient pulse for both SiGe HBT models under the LET = 10 MeV-cm^2/mg ion strike, the simulated collector transient waveforms against a linear y-axis is shown in Fig. 4.12. The simulated *pnp* SiGe HBT exhibited a reduced peak transient magnitude, reduced FWHM, and an approximate 3× reduction in collected charge, agreeing with the experimental results reported earlier and supporting our original hypothesis that the n-well isolation layer is responsible for the *pnp* SiGe HBT's inherent SET improvement.

Fig. 4.13 shows the changes in the *pnp* collector transient waveform for three different ion strikes (LET = 0.5, 1, and 2 MeV-cm^2/mg) across multiple n-well doping concentrations. As the dopant density of the n-well isolation layer is increased, the ion-shunt transient peak is shown to monotonically increase, while the transient

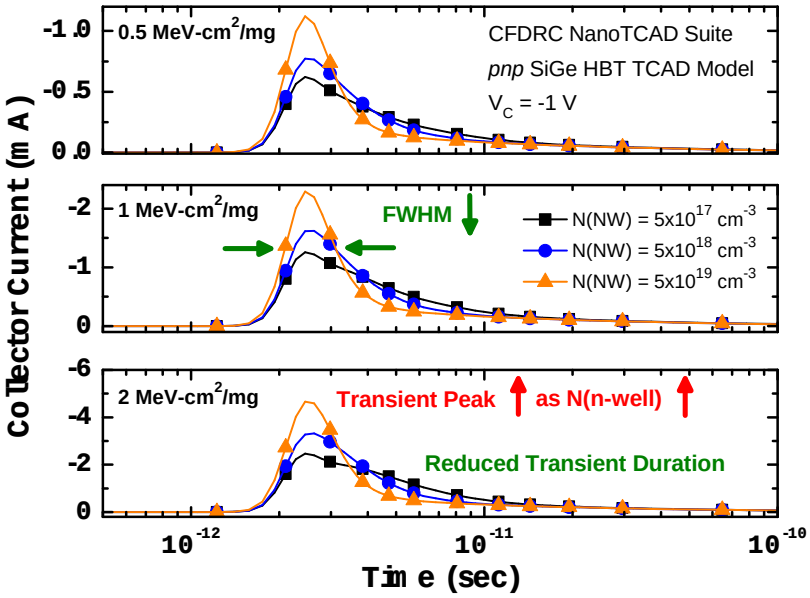


Figure 4.13: Simulated collector current transients for the bulk *pnp* HBT operating under a forward-mode, off-state bias across multiple ion-strike LETs and n-well doping densities.

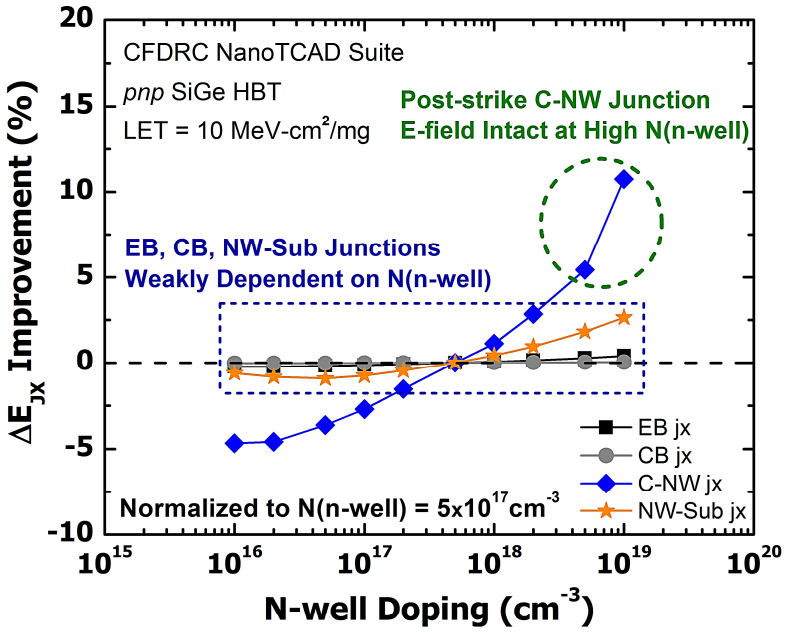


Figure 4.14: Improvement in post-strike junction E_{FIELD} for the *pnp* SiGe HBT under a LET = 10 MeV-cm^2/mg ion strike across multiple n-well doping concentrations. All values have been normalized to the the N(n-well) = 5×10^{17} cm^{-3} *pnp* ion-strike simulation.

waveform displays a reduction in FWHM and overall transient duration. To better understand how the ion-strike junction dynamics are affected by n-well dopant density, the post-strike change in the electric field for the emitter-base, collector-base, collector n-well, and n-well substrate junctions are shown in Fig. 4.14, where ΔE_{JX} is defined as the percentage decrease in the junction E_{FIELD} immediately after an ion strike (i.e., during the ion-shunt current regime). This figure of merit captures the extent of which each junction breaks down from the large post-strike influx of charge carriers. In order to facilitate comparisons between ion strikes, this figure of merit has been normalized to the N(n-well) = 5×10^{17} cm^{-3} *pnp* ion-strike simulation, resulting in "ΔE_{JX} improvement," as seen in Fig. 4.14. A positive shift in "ΔE_{JX} improvement" indicates that the internal electric fields at that particular junction are less affected by the passage of a heavy ion. Alternately, a negative shift indicates a greater breakdown of the junction E_{FIELD} and subsequent space-charge region.

As expected the emitter-base and collector-base junctions are unaffected by the

n-well doping concentration. The n-well substrate junction is weakly dependent since the junction E_{FIELD} is limited by the doping concentration of the lower-doped side of the junction (which in this case is the p-substrate). The collector n-well junction, on the other hand, is very sensitive to the n-well dopant density and Fig. 4.14 shows an increase in the post-strike residual electric field at this junction for elevated n-well doping concentrations. The greater electric field at this junction is able to more effectively sweep excess charge carriers into the collector and n-well terminals and decrease the time it takes for the collector n-well depletion region to re-form, resulting in the reduced FWHM seen in both the experimental and simulation datasets. Once this junction re-establishes, the collector terminal is effectively isolated from the large carrier concentrations in the thick bulk substrate, leading to the reduced diffusion tail seen in Fig. 4.11. This isolation between the output terminal (collector) and the bulk substrate is largely responsible for the observed reductions in collected charge at the collector terminal. The reduction in collector collected charge as a function of collector

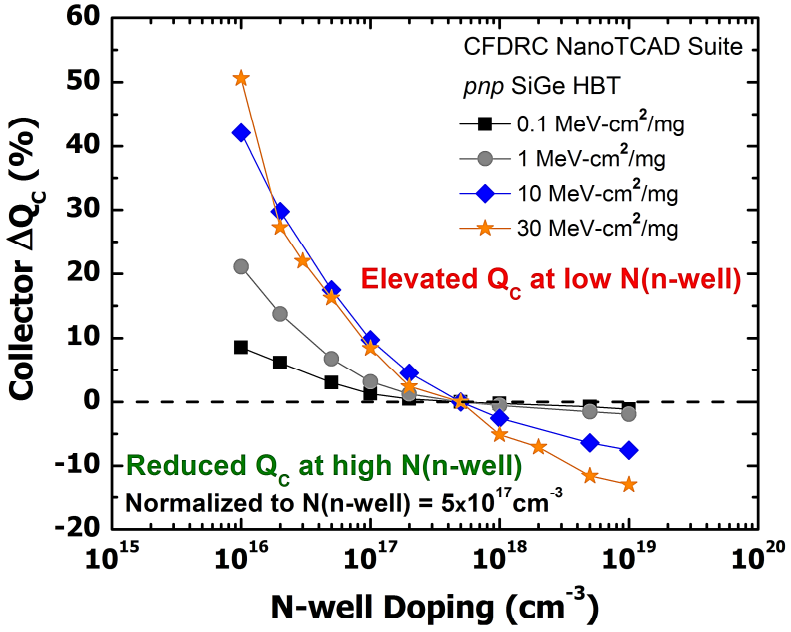


Figure 4.15: Change in collected charge at the collector terminal for the *pnp* SiGe HBT across multiple ion-strike LETs and n-well doping concentrations. All values have been normalized to the the N(n-well) = 5×10^{17} cm^{-3} *pnp* ion-strike simulation.

doping across ion-strike LET is shown in Fig. 4.15. As in Fig. 4.14, the collected charge has been normalized to the N(n-well) = 5×10^{17} cm^{-3} *pnp* ion-strike simulation. As n-well doping concentration is decreased below N(n-well) = 5×10^{17} cm^{-3}, Fig. 4.15 shows a sharp increase in collected charge at the collector terminal, especially at higher ion-strike LETs, which confirm our previous conclusions that the n-well isolation layer is driving the *pnp* SiGe HBT's SET improvement. However, it should be noted that the improvement in collected charge become less substantial for n-well dopant densities above 5×10^{17} cm^{-3} since the incremental collector n-well junction E_{FIELD} is decreased as the n-well doping concentration approaches the subcollector doping concentration.

The previous simulations have shown that the n-well layer inherent to *pnp* SiGe HBTs leads to the transient duration and collected charge improvements observed during pulsed-laser TPA testing. Since all previous ion-strike simulations were for an ion passing through the center of the HBT material stack, it is pertinent to extend our TCAD analysis to include ion strikes that pass outside but within the vicinity of the SiGe HBT. Theoretically, the n-well should isolate the HBT output from most of the

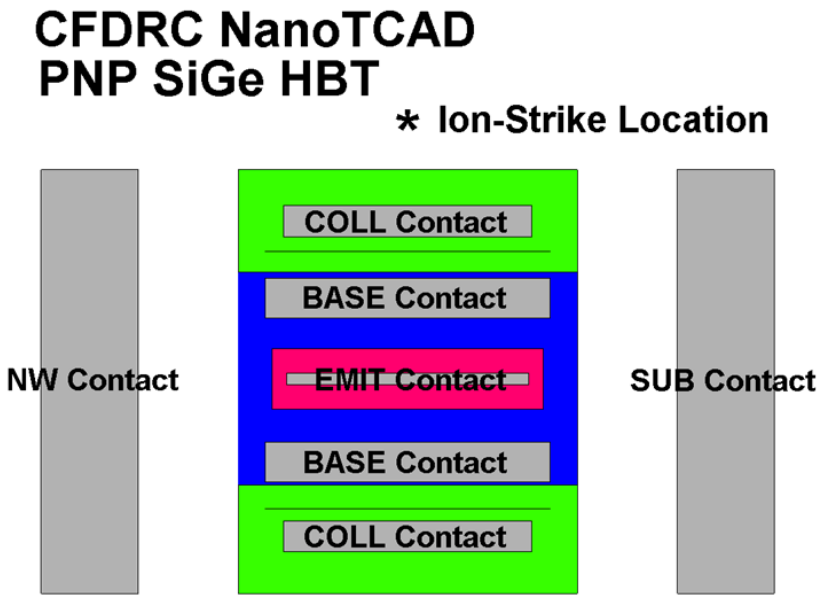


Figure 4.16: Top-down view of the 3-D model developed within CFDRC NanoTCAD. The off-center strike location, located 0.5 μm away from the HBT device volume has been annotated.

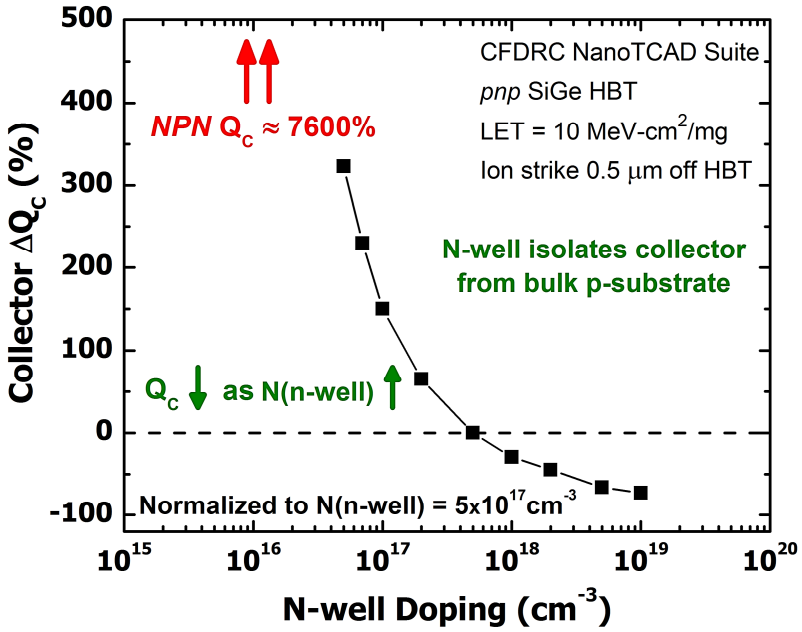


Figure 4.17: Change in collected charge at the collector terminal for the *pnp* SiGe HBT under a LET = 10 MeV-cm^2/mg ion strike across multiple n-well doping concentrations. All simulations are for an ion strike into the p-substrate, located 0.5 μm away from the *pnp* SiGe HBT. All values have been normalized to the the N(n-well) = 5$\times$10^{17} cm^{-3} *pnp* ion-strike simulation.

deposited charge in the p-substrate, leading to the significant decrease in sensitive area reported earlier. In order to verify these experimental results, additional ion-strike TCAD simulations were performed for a LET = 10 MeV-cm^2/mg ion strike 0.5 μm away from *pnp* SiGe HBT. An illustration detailing a top-down view of the 3-D model and the strike location for all off-center ion strikes is shown in Fig. 4.16. As in previous simulations, the n-well doping concentration was varied to ascertain the effect of this parameter on the SET response and the simulation results were normalized to the N(n-well) = 5$\times$10^{17} cm^{-3} ion-strike case. From Fig. 4.17, the *npn* SiGe HBT collects approximately 7600% more charge than the *pnp* SiGe HBT, agreeing with the TPA results shown in Fig. 4.7. If these same simulation results are normalized with respect to the *npn* HBT, then the *pnp* SiGe HBT exhibits a 98.7% drop in collected charge at the collector terminal. As with device-incident ion strikes, ΔQ_c is very dependent on the n-well doping concentration. The TCAD simulations presented in this section

support the importance of n-well geometry and doping on the *pnp* SET response and suggest that *pnp* SiGe HBTs should offer SEE benefits across multiple bulk C-SiGe technology platforms. However, it should be noted that raising the doping level of the n-well isolation layer can negatively impact the dynamic performance of the *pnp* SiGe HBT due to elevated device parasitics.

4.5 Summary

The pulsed-laser TPA SET results for a third-generation C-SiGe BiCMOS process were presented, where the bulk *pnp* SiGe HBT exhibited significant improvements in sensitive area as well as a reduction in overall transient duration and collected charge at the output (collector) terminal. 3-D TCAD ion-strike simulations agree with the experimental findings and show that the n-well isolation layer present in the vertical structure of the *pnp* HBT is the primary mechanism driving the observed SET improvement. The device-level improvements highlighted in this report suggest that precision analog, RF/mm-wave, and high-speed digital circuits utilizing the bulk high-performance *pnp* should benefit from an improved SEE response. As technology scaling drives greater improvements in device performance for both *npn* and *pnp* SiGe HBTs, fully-*pnp* circuits may become an effective strategy for developing SEE-tolerant, bipolar electronics.

CHAPTER 5

SEE MODELING TECHNIQUES FOR A SIGE-BASED LOW-NOISE AMPLIFIER

5.1 Motivation

As applications such as global telecommunications, radiometry, and satellite navigation (GPS) incorporate advanced, high-frequency in-orbit electronics, it is pertinent to understand how these RF systems operate within a dynamic and potentially hazardous environment. The ability to accurately capture and model complex transient mechanisms at the circuit and system level is of great interest to the radiation effects community. Prior work on digital test structures revealed a strong dependence between simulation approach (current injection, mixed-mode, etc.) and simulation accuracy [106]. Valid SEE modeling techniques that can accurately capture the internal voltage/current transient dynamics within individual RF blocks are a critical tool in the future development of low-cost, SEE-tolerant RF transceiver systems. Leveraging these tools to understand the impact of external packaging parasitics on the system-level SEE response is of particular importance. Therefore, this investigation has two major goals: 1) to provide an understanding of how circuit and system-level parasitics affect SEE within RF electronics, and 2) to assess the impact of various transient TCAD modeling approaches on simulation fidelity for SEE in space-based radar and communications systems, and thereby recommend best practices for the space community.

5.2 L-Band (1 – 2 GHz) SiGe Low-Noise Amplifier

To expand our understanding of transient phenomena within high-frequency circuits, an L-band (1 – 2 GHz), SiGe-based low-noise amplifier (LNA) was designed for transient characterization. A simplified schematic of the LNA is shown in Fig. 5.1, where the three primary locations of SiGe HBTs are highlighted for clarity. The LNA was designed using a third-generation, 130 nm SiGe BiCMOS process (IBM 8HP), providing unity current gain (f_T) and maximum oscillation (f_{MAX}) frequencies of 200 and 285 GHz, respectively [79]. This SiGe-based LNA utilizes a cascode topology with a common-emitter (CE) stage and a common-base (CB) stage, leading to higher power gain and improved reverse (output to input) isolation. The LNA also has a SiGe HBT and resistor network (current mirror) that sets the *dc* base-emitter voltage for the common-emitter stage. Table 5.1 lists several relevant performance metrics for this SiGe LNA. This circuit has several important characteristics that are well suited for radiation testing. The low operating frequency (≈ 1.24 GHz) reduces the impact of high-frequency packaging parasitics (wirebond inductance, on-board transmission

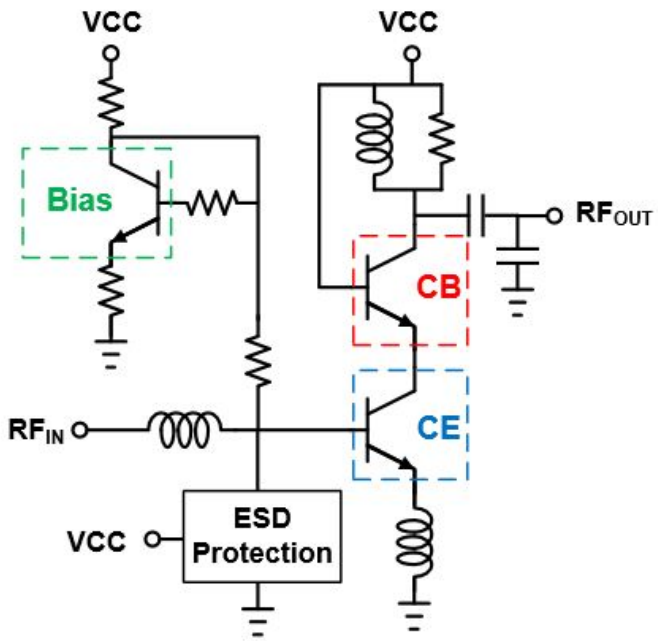


Figure 5.1: Simplified schematic diagram of the L-band SiGe LNA.

Table 5.1: Simulated performance of the SiGe L-band LNA near L1 (1575 MHz) and L2 (1227.60 MHz) GPS frequencies.

Design Parameter	@ 1.2 GHz	@ 1.5 GHz
Input Return Loss	18.4 dB	28.2 dB
Power Gain	26.0 dB	23.1 dB
Reverse Isolation	38.7 dB	40.6 dB
Output Return Loss	19.1 dB	10.4 dB
Noise Figure	1.25 dB	1.49 dB

line resistance, SMA cabling capacitance, etc.), thus minimizing signal degradation within an SEE testing environment. The simple LNA topology also reduces simulation overhead, thereby improving the numerical convergence of ion-strike simulations. However, compared to digital and analog circuits, the required TCAD model decks for devices within a high-frequency amplifier must accurately model the dynamic performance of the SiGe HBT, allowing us to ascertain the effects of small-signal *ac* modeling on circuit-level ion-strike simulations. This L-band LNA was designed for emerging Global Position System (GPS) applications (MEO orbit) and is representative of high-performance amplifiers used in these GPS systems.

5.3 Pulsed-Laser TPA Testing

Laser-induced transients were measured at the U.S. Naval Research Laboratory (NRL) using the established two-photon absorption SEE characterization system. A full system description is provided in Section 3.4. The LNA test circuits were packaged and wire-bonded onto a custom-designed printed circuit board (PCB) that left the back substrate surface exposed for irradiation. Special care was taken to minimize bond wire lengths in order to prevent excess parasitic inductance from disturbing circuit functionality. To reduce the impact of supply noise from affecting circuit performance, surface-mount technology (SMT) decoupling capacitors were soldered between the *dc* supply lines and the shared ground plane. SMT capacitor values of 0.1 μF, 1 μF, and

10 μF were used to ensure a broadband short to ground. The laser pulse energy (PE) for all transient data is 2.9 nJ, unless otherwise noted. All 2-D raster measurements were collected with a step size of 0.5 μm, unless otherwise noted.

2-D raster scans were performed under a *dc-only* operating condition (no RF input) while monitoring the circuit terminals for any inherent laser-induced, device-level transients, leading to the output transient plot shown in Fig. 5.2 for the common-emitter stage (CE devices). Since a low-noise amplifier functions as the first stage of an RF receiver, any perturbations on the output can become amplified by subsequent gain stages (RF mixer, VGA, etc.), and therefore, LNA output SETs are of the utmost concern. The CE devices are composed of parallel SiGe HBTs in order to meet linearity requirements, with a small ($\approx$ 22 Ω) n+ diffusion resistor between the collector terminals of each SiGe HBT to improve stability. Fig. 5.2 shows that the CE devices are highly sensitive to SEE and can drive large current transients at

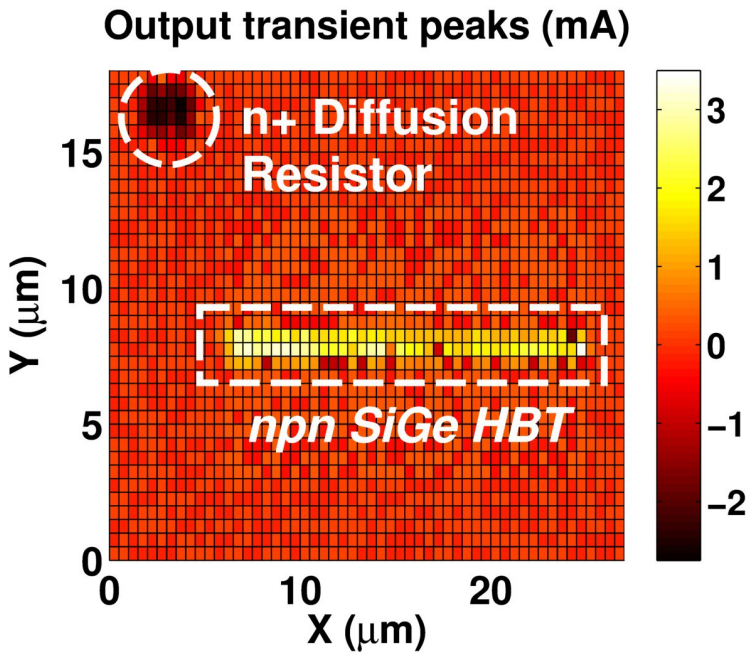


Figure 5.2: 2-D LNA output transient peaks for a strike to a common-emitter device under *dc-only* operating condition.

the LNA output because the common-base devices (CB devices) act as a near-unity-gain current buffer (current gain $\approx$ 0 dB). It is also important to note that since the n+ diffusion resistor acts as a reverse-biased p-n junction with the surrounding p-substrate, it was highly effective at collecting laser-induced charge carriers with transient peaks close to that of a SiGe HBT strike.

The time-domain transient waveform and frequency spectrum for a CE device strike are shown in Fig. 5.3, exhibiting large current transient peaks and spurious tones across the L-band (GPS) frequencies. This observation is particularly important to an RF transceiver since traditional band-pass filtering techniques subsequent to the LNA gain stage will be unable to completely reject these spurious components, thereby potentially corrupting the original RF signal. Furthermore, the addition of spurious frequency components at the LNA output can generate conversion issues when these signals are passed to and down-converted by the RF mixer. While transient signals under a *dc-only* operating condition provide a basic understanding of internal voltage/current dynamics under SEE, it is relevant and necessary to analyze

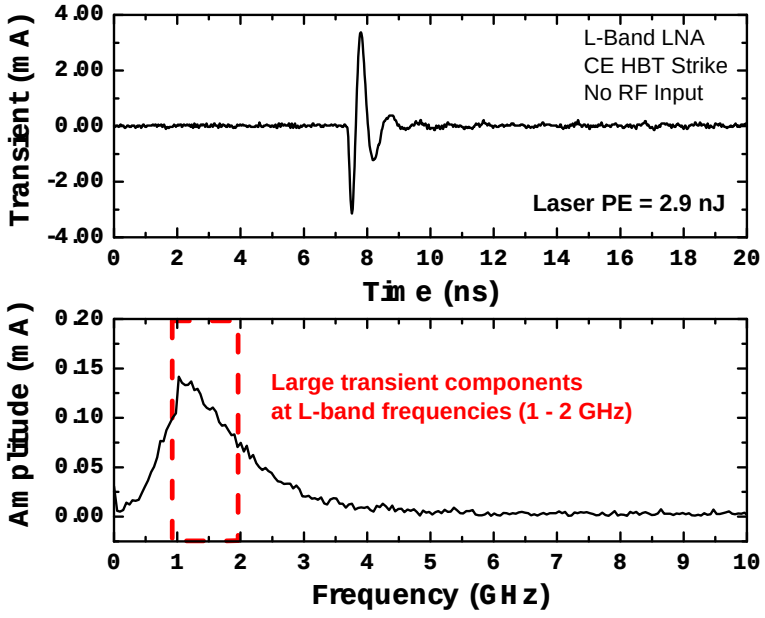


Figure 5.3: Measured output current transients and frequency spectra for a strike to a common-emitter device under *dc-only* operating condition.

how SiGe HBT-driven SETs affect the LNA RF output signal. Therefore, transient waveforms for the SiGe LNA with a 1.5 GHz RF input signal were captured. The RF input power was varied from -40 dBm to -20 dBm to provide comparison points and ascertain whether the signal strength will affect the SEE sensitivity of the LNA.

After verifying that the most sensitive location for SET corresponded to emitter-center of the SiGe HBT material stack (emitter/base/collector), transient waveforms were captured at this fixed position across input power. From Fig. 5.4, heavy amplitude and frequency distortions are seen at the output terminal at low RF input power (-40 dBm). The frequency spectrum in Fig. 5.5 indicates a 10× increase at frequencies near the fundamental carrier frequency, which is clearly undesirable. By translating these frequency spectra on a logarithmic scale, a 20 – 40 dB increase of side-band signal power is observed in Fig. 5.6, which raises potential concerns for digital data modulated within the RF carrier signal. At elevated input power (-20 dBm), the time-domain distortions are less significant since the peak-to-peak output swing of the amplified sinusoidal signal is now 5× larger than the laser-induced transient

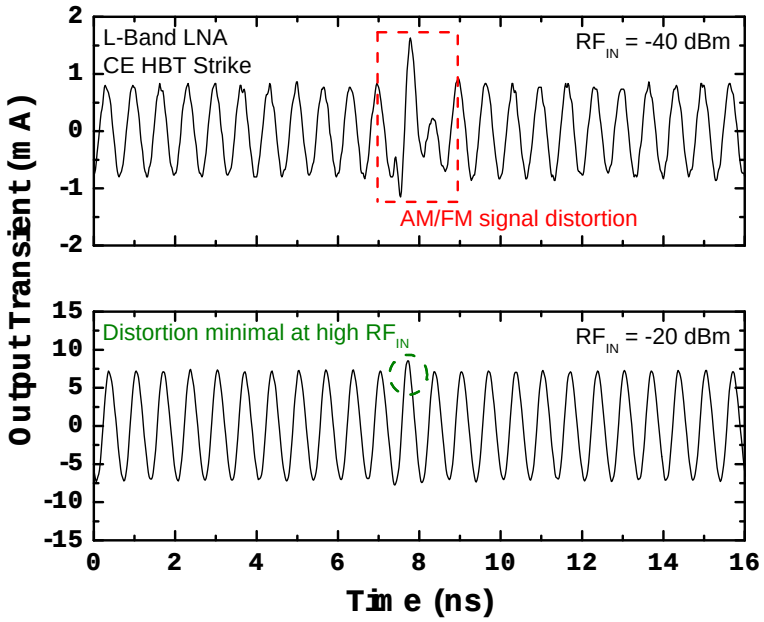


Figure 5.4: Measured output current transients for a CE strike under low (-40 dBm) and high (-20 dBm) RF input power.

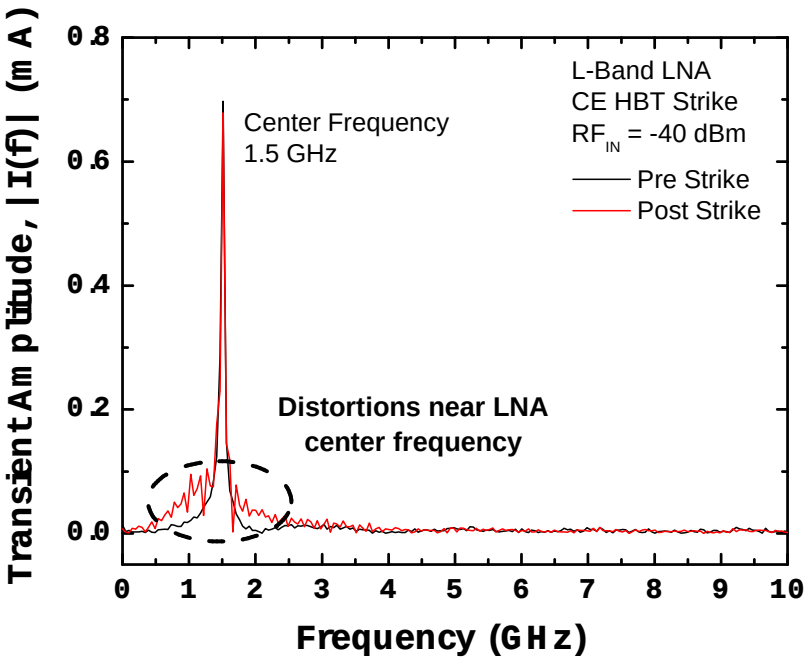


Figure 5.5: Frequency spectra detailing LINEAR transient amplitude components for a CE strike and an RF input power of -40 dBm.

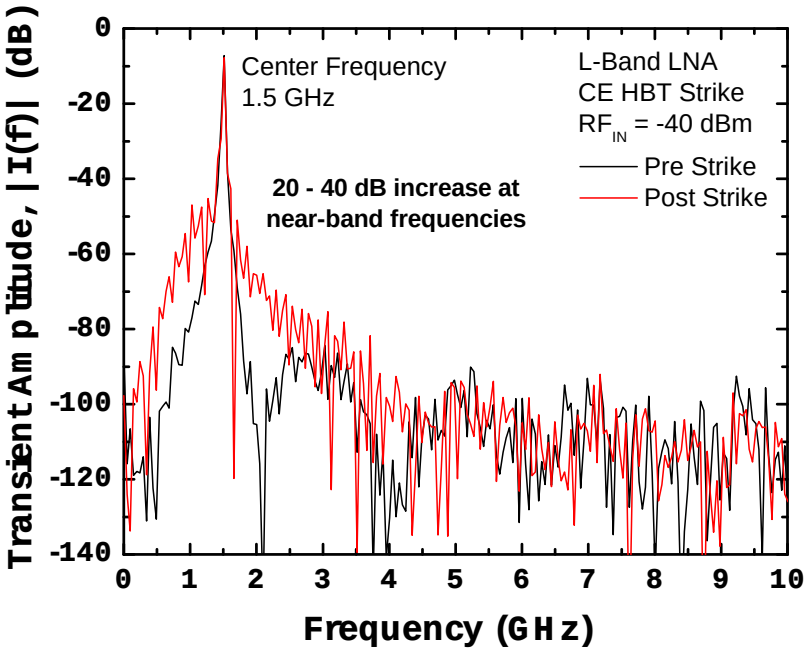


Figure 5.6: Frequency spectrum detailing LOG transient amplitude components for a CE strike and an RF input power of -40 dBm.

peak, but since these amplifiers are intended to boost weak signals from the feed-line of an antenna, these current transients and resultant distortions are a legitimate cause for concern.

2-D raster scans were also performed for the common-base (CB) SiGe HBTs under a *dc-only* operating condition, resulting in the output transient plot shown in Fig. 5.7, where a significant reduction ($\approx 10\times$) in output transient peaks is observed at the LNA output terminal. The simplified circuit schematic in Fig. 5.1 can help explain the reason for the reduction in SET sensitivity for a CB device strike. To the CB SiGe HBT, the CE devices essentially act as a tail current source, which helps to reject the large emitter transient coming from these devices. Therefore, the laser-induced charge carriers within the CB device must travel through another signal path or are left to recombine. Previous work has shown that the large transient peak within bipolar devices is attributed to the "ion shunt" effect [107,108], which leads to a large drift component induced by the electrical breakdown of the emitter-base, collector-base, and collector-substrate junctions within the bulk SiGe HBT [1,3]. Since the CE

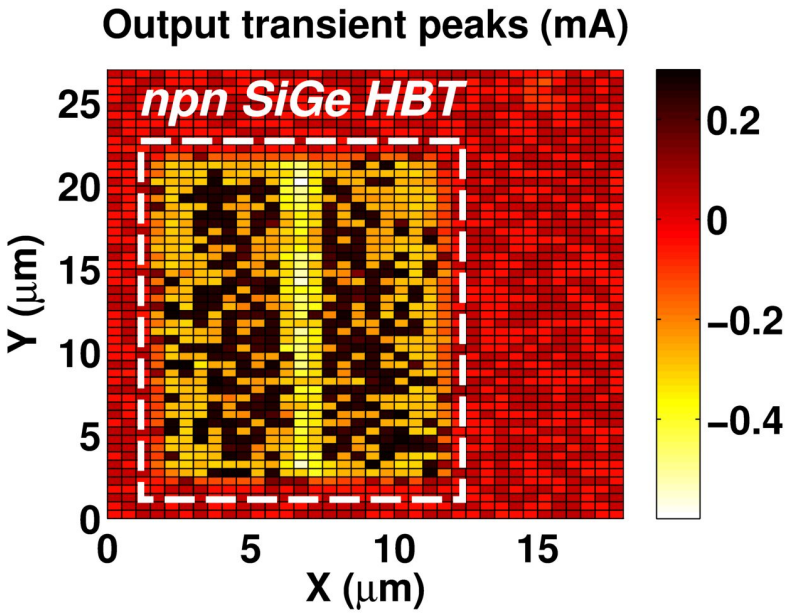


Figure 5.7: 2-D LNA output transient peaks for a strike to a common-base device under *dc-only* operating condition.

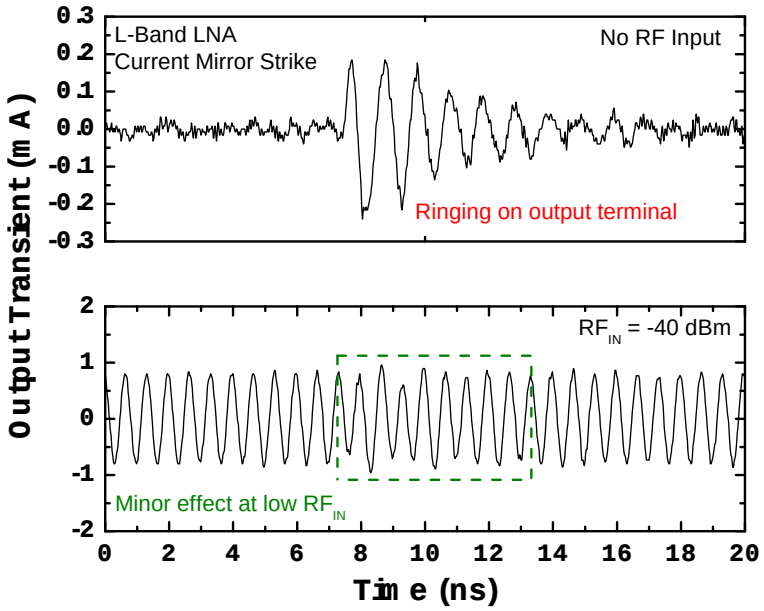


Figure 5.8: Measured output current transients for a strike to the bias circuit under *dc-only* and low RF input operating conditions.

stage rejects this emitter transient, a majority of the carriers are left to recombine, resulting in the minimized transients detected at the output terminal.

Similar 2-D scans were performed for the current mirror (CM) voltage biasing SiGe HBT under a *dc-only* operating condition. However, the recorded output transients were minor and on the same order as the noise floor of the pulsed-laser system. For brevity, these raster scans have not been included in the present discussion. Fig. 5.8 shows the output transient waveforms for a CM device strike under *dc-only* and low RF input power (-40 dBm). Although a CM strike exhibits a small transient with extended ringing at the output terminal, these perturbations cause minimal distortion to the carrier signal and should not pose a major SEE concern.

5.4 3-D TCAD Modeling and Simulations

To expand our understanding of how circuit feedback and other design constraints affect SET within RF/mm-wave circuits and systems, TCAD ion-strike simulations were performed for the L-band SiGe LNA. A 3-D TCAD model of a third-generation

SiGe HBT was developed using the aforementioned NanoTCAD software suite developed by CFD Research Corporation (CFDRC NanoTCAD). The 3-D HBT model was *dc* and *ac* calibrated to the Cadence IBM process design kit (PDK) compact model to ensure numerical convergence in subsequent circuit-level, mixed-mode ion-strike simulations. In order to match the elevated current densities throughout a SEE and guarantee the closest match to experimental TPA results, the model was scaled to the same device dimensions (0.12 μm $\times$ 18 μm) of the SiGe HBTs utilized in the test circuit.

The single-event response at the circuit level depends heavily on topology due to feedback effects and for certain circuits, dynamic biases that evolve on the same time scale as radiation-induced transient current pulses. Moreover, the importance of addressing these modeling issues grows as advanced lithographic scaling drives circuit response times into picosecond and sub-picosecond operating regimes [122]. As a result, clear guidelines must be established as to which SET modeling approaches are valid for various conditions (e.g., circuit topology, technology node, device geometry, environment, etc). Traditional "current injection" simulations utilize a decoupled approach where a set of transient waveforms representing the device-level SEE response are injected into the surrounding circuit via ideal, independent current sources [123,124]. These transient waveforms can be represented by simple analytical expressions (double-exponential, trapezoidal, etc.) or complex piece-wise waveforms obtained from device-level, ion-strike simulations [125]. Since ideal sources inject these current waveforms without any feedback from the circuit itself, large discrepancies can occur between measurement and simulation. The reader is directed to the previous studies for more information on the limitations of traditional, current-injection simulation approaches.

The work flow from electronic design to packaging and pulsed-laser testing introduces a large number of external parasitics to the device under test (DUT) due to the

wirebonds, PCB trace parasitics, SMA connector losses, cabling capacitances, etc. Previous studies have shown a strong dependance of internal and external parasitics to the efficacy of radiation event modeling with respect to device and analog circuit single-event transients (ASETs) [109, 126]. Since package parasitics can have a strong impact on the overall performance of high-frequency RF circuits, they may have a similar effect on radiation-induced transients within these circuits, particularly with how the SET manifests in the frequency domain. Radiation-induced side-band components, such as the frequency signature observed in Fig. 5.6, are relevant for RF system engineers, but the ability of ion-strike simulations to accurately capture these signatures remains largely unknown. Therefore, the circuit-level modeling techniques presented will provide a way to visualize these issues and determine their importance in accurate modeling.

5.4.1 Feedback and Packaging Effects on Circuit-level SEE Modeling

Fully-coupled mixed-mode simulations of the SiGe L-band LNA were leveraged to ascertain how circuit feedback and packaging parasitics affect circuit-level transient simulation fidelity. For all simulations, a single SiGe HBT was replaced with the 3-D nanoTCAD model deck and subjected to a heavy-ion strike across multiple linear energy transfers (LET = 1 – 10 MeV-cm^2/mg). All ion-strike simulations are normal to emitter-center since this represents the worst-case scenario where the heavy ion passes through all three sensitive junctions of the *npn* SiGe HBT (emitter-base, collector-base, and collector-substrate). A linear energy transfer (LET) of 10 MeV-cm^2/mg was selected for the high-energy case since a significant majority of incident particle flux within orbital environments correspond to ion strikes at these lower LET values [87, 127].

Simulated LNA (*dc-only*) output transients for a common-emitter and common-base device strike (i.e., a heavy-ion strike to a SiGe HBT in the LNA CE stage or

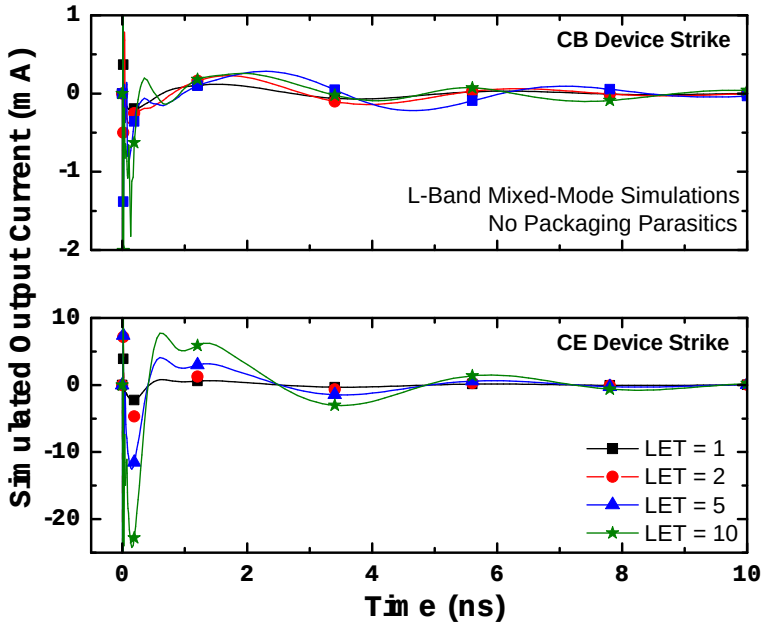


Figure 5.9: Overlaid simulations of LNA output waveforms for a CE and CB device strike across LET = 1, 2, 5, 10 MeV-cm^2/mg.

LNA CB stage) across four different ion-strike LETs (1, 2, 5, and 10 MeV-cm^2/mg are shown in Fig. 5.9. These initial simulations do not include any external parasitics to reduce numerical complexity and provide a baseline for future simulations. There are several key issues that can be observed. For the CB device strike, the peak transient magnitudes are much larger than the measured TPA results shown in Fig. 5.7. While the minimum and maximum Y-axis values are set to -1 mA and 1 mA to improve visibility, the actual minimum and maximum transient magnitude for the LET = 10 MeV-cm^2/mg case was approximately -15 mA and 7 mA, respectively. For the CE device strike simulations, the output transient shape and duration do not match the recorded *dc-only* transient waveform in Fig. 5.3. These results indicate that the external parasitics inherent to the TPA measurement setup, such as the packaging capacitance (decoupling capacitors), bond wire resistance and inductance, and SMA cable losses, may have a strong impact on the predicted single-event transients.

To investigate this issue further, another simulation deck incorporating the aforementioned parasitics was developed for mixed-mode analysis. Ideal decoupling capacitors of 0.1 μF, 1 μF, and 10 μF were added between the *dc* voltage bias line (VCC) and common ground. An ideal impedance (R = 275 mΩ, L = 1.8 nH) was inserted after all circuit terminals to represent the bond wire parasitics between the test circuit and PCB test board. Two-port circuit blocks (N2P) were inserted between the bond wires, *dc* biasing sources, RF input source, and an oscilloscope load impedance (output terminal). The two-port S-Parameters (S2P) for the Fairview Microwave 36-inch SMA cables used in the TPA experiment were characterized using a Vector Network Analyzer (VNA) and associated laboratory equipment. The measured S2P files were then loaded into the N2P blocks to represent all SMA cabling used in the experimental setup.

Overlaid LNA output transients for an ion strike to the CE device (LET = 1 MeV-cm^2/mg) for both the LNA schematic without external parasitics (Fig. 5.9)

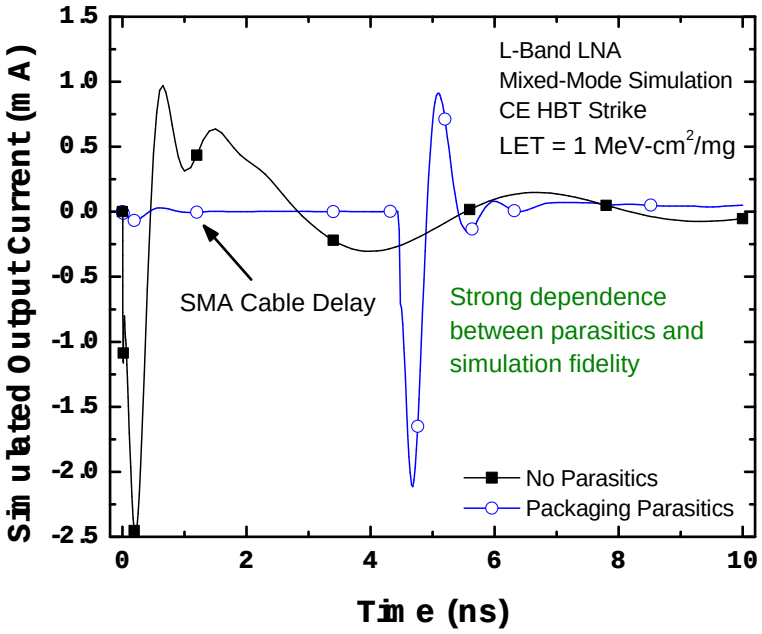


Figure 5.10: Overlaid simulations of output waveforms for the LNA without and with external parasitics under a low-energy ion-strike to a CE device (LET = 1 MeV-cm^2/mg).

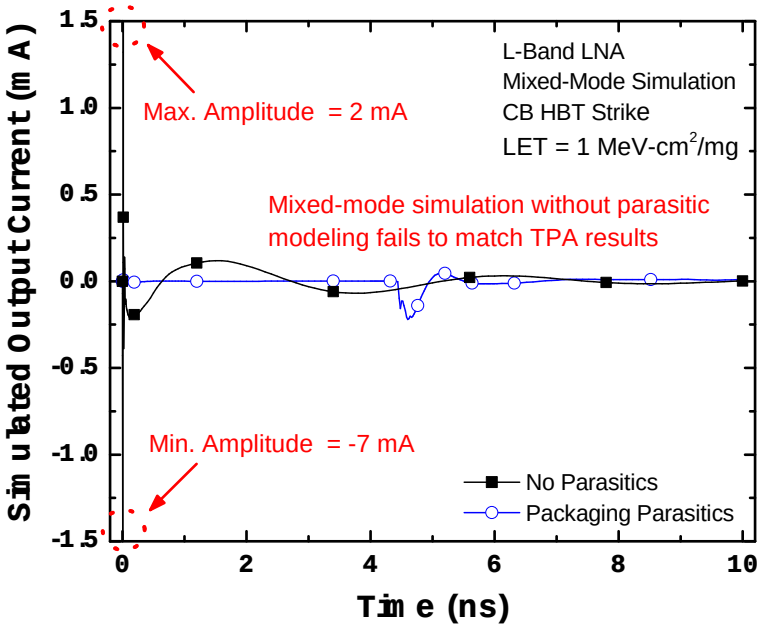


Figure 5.11: Overlaid simulations of output waveforms for the LNA without and with external parasitics under a low-energy ion-strike to a CB device (LET = 1 MeV-cm^2/mg).

and with external parasitics are shown in Fig. 5.10. As previously discussed, the mixed-mode simulation for the circuit without parasitics fails to match the observed TPA transients. The "improved" circuit (i.e., with packaging parasitics), exhibits an enhancement in its ion-induced SET response, with transient magnitude, pulse width, and duration closely matching those from previous experimental results. Fig. 5.11 shows a similar comparison for an ion strike to a CB device, where the Y-axis was reduced to improve visibility of the "improved" circuit simulation. Although there is significant clipping of the transient waveform for the circuit without parasitics, the minimum and maximum transient magnitudes have been annotated. From this figure, it is apparent that the circuit without parasitics fails to capture the feedback mechanisms (current shunt rejection) observed during pulsed-laser testing, since the transient magnitudes are significantly larger than those for a CE strike. The "improved" circuit simulation, however, exhibits a strong reduction in transient magnitude when

compared to a CE strike, agreeing with experimental results and confirming the importance of parasitic modeling on SET simulation fidelity. It should be noted that the incorporation of external parasitics into the mixed-mode simulation deck does result in a significant increase in numerical complexity and simulation time (≈ 60 %), with the "improved" circuit, i.e. with external parasitics, requiring approximately 89 hours to complete an ion-strike simulation (LET = 1 MeV-cm^2/mg) compared to 55.5 hours for the standard circuit without parasitics. However, this computational overhead is a minimal cost to pay for the improved accuracy and reliability of the results.

All previous ion-strike simulations have been for a *dc-only* case without an RF input signal. However, it is pertinent to assess whether mixed-mode simulations accurately capture the post-strike dynamics in the frequency domain since subsequent stages in an RF transceiver, such as an RF mixer, can be highly sensitive to any frequency perturbations. The ability for mixed-mode simulations to accurately capture

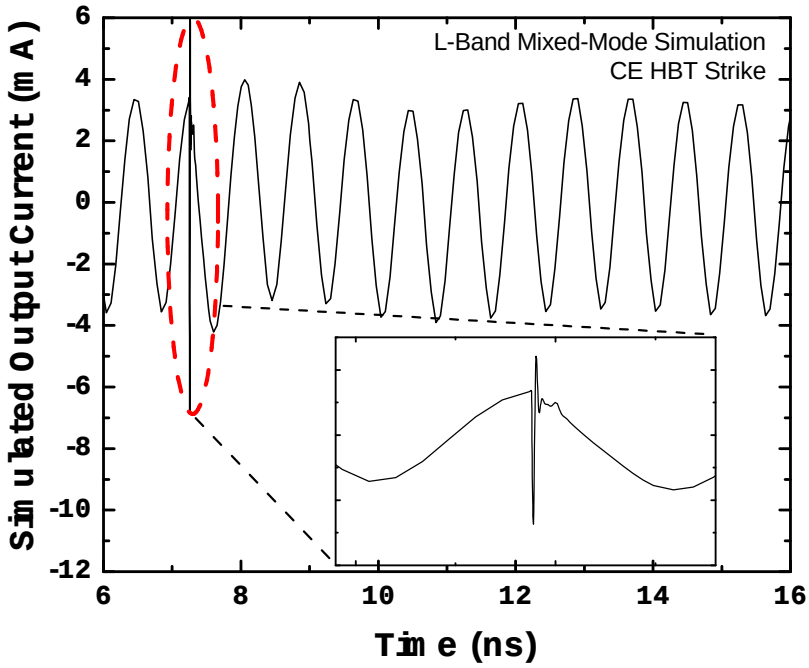


Figure 5.12: Simulated LNA output transients for the circuit with RF input = -40 dBm under an ion-strike of LET = 1 MeV-cm^2/mg.

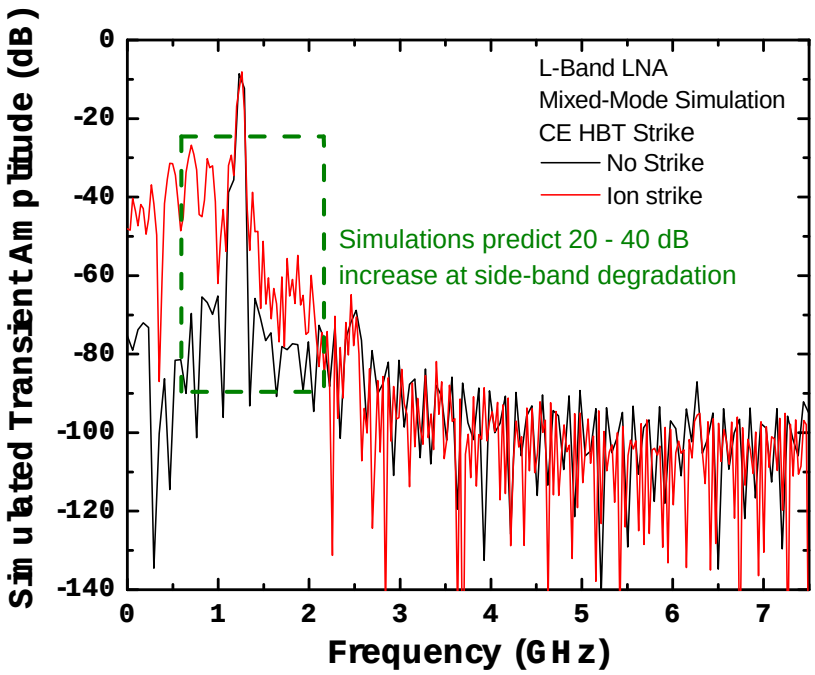


Figure 5.13: Simulated LNA frequency spectrum detailing LOG transient amplitude components for a CE strike and an RF input power of -40 dBm.

these phenomena can serve as a useful tool for system engineers to model the interactions between sub-systems and predict possible issues with respect to SEE. Therefore, an ion-strike simulation was performed for the "improved" circuit at an ion-strike LET = 1 MeV-cm^2/mg and RF input signal (1.25 GHz, -40 dBm). Fig. 5.12 shows the ion-induced transient where amplitude and frequency distortions to the sinusoidal output signal are clearly visible.

To better visualize the simulated SEE frequency response of this circuit, the time-domain waveforms with an ion strike (Fig. 5.12) and without an ion strike were transformed to the frequency domain via FFT and overlaid, resulting in the transient magnitude plot shown in Fig. 5.13. Elevated amplitudes adjacent to the fundamental frequency (1.25 GHz) are seen for the ion-strike case, resulting in a 20 – 40 dB increase of side-band signal power. These observations agree with the TPA-induced frequency spectra shown in Fig. 5.6, thereby demonstrating the capability of CFDRC MixCAD simulations to reliably model the complex transient phenomena within high-frequency

circuits and systems. The amplitude discrepancies toward lower frequencies suggest the present simulation is lacking a component that attributes to signal loss, such as the Southwest SMA end launchers. These secondary components were removed from the sinusoidal simulation to reduce computational overhead since the current circuit requires approximately one week to complete a single ion-strike simulation. The close match at higher frequencies, however, indicates the present simulation deck has accurately modeled the major parasitic impedances (parasitic resistances, capacitances, inductances) within the SiGe LNA.

5.5 Summary

An L-band (1 – 2 GHz) low-noise amplifier (LNA) implemented in a third-generation, bulk SiGe BiCMOS process was presented with a focus on the pulsed-laser TPA SET response. The transient response of the LNA was shown to be highly dependent on strike location due to loading, external parasitics, and internal feedback effects. Circuit-level, ion-strike simulations exhibited a strong dependence on parasitic modeling and transient simulation approach, revealing a fundamental trade off between simulation fidelity and computational overhead. CFDRC mixed-mode (CFDRC MixCAD) simulations which incorporated key packaging parasitics displayed excellent agreement against experimental datasets, confirming that these approaches can accurately model the complex transient mechanisms within high-frequency circuits. Therefore, the approaches outlined here can serve as a useful tool for system engineers to understand transient processes within complex systems and develop effective mitigation strategies against single-event effects.

CHAPTER 6

IMPACT OF SEMICONDUCTOR TECHNOLOGY SCALING ON THE SEE RESPONSE OF SIGE HBTS

6.1 Motivation

The need for affordable, high-performance electronic systems within RF/mixed-signal applications has driven significant research and innovation in the semiconductor industry. In particular, silicon-based technologies have witnessed continuous levels of advancement in order to boost performance and maintain strong economies of scale, with current CMOS technologies at the 14-nm lithographic node and 10-nm technologies on the horizon. While alternative semiconductor platforms, such as Gallium Arsenide (GaAs), Gallium Nitride (GaN), and Indium Phosphide (InP), provide significant advantages for specific applications, silicon is still the preferred platform due its low cost, high reliability, and ease of manufacturing. Semiconductor process scaling has driven remarkable improvements in device performance (for both FET and bipolar), thereby allowing silicon-based technologies to match or outperform other semiconductor technologies. However, lateral shrinking of silicon technologies is approaching a physical limit and many "vanilla" silicon processes are unable to provide the performance necessary for high-speed digital and RF communication systems, which provides an opening that is ideally suited for the expanded capabilities of SiGe BiCMOS technologies.

Fig. 6.1 shows the schematic cross-sections for a representative first-generation and third-generation SiGe HBT, highlighting the differences between these platforms.

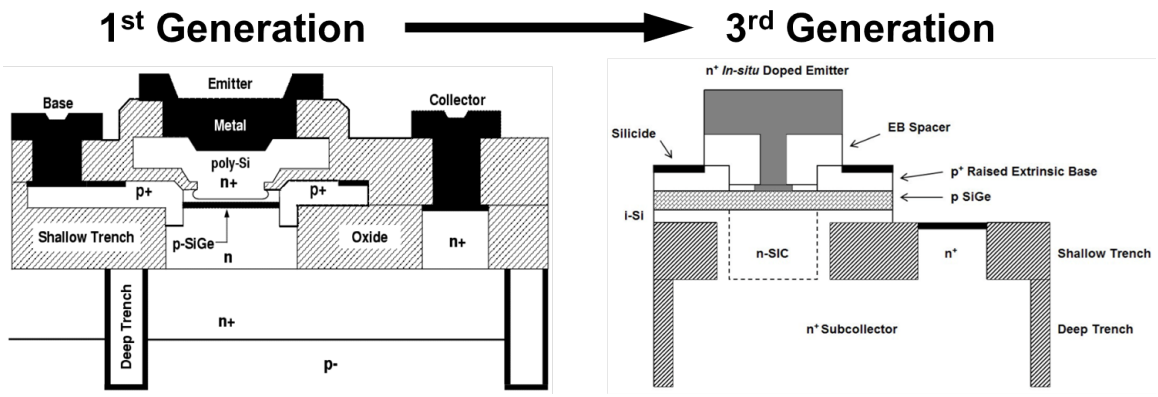


Figure 6.1: Schematic cross-sections for a first-generation and third-generation SiGe HBT, highlighting the differences between these technologies (after [17]).

While early SiGe technologies can be "non-self-aligned" to reduce overhead and complexity in the cleanroom process flow, it is increasingly common for current generations to have a "self-aligned" architecture. Self-alignment implies that the transistor extrinsic base is self-aligned to the emitter opening during fabrication, an important feature that can reduce the intrinsic and extrinsic parasitics and improve device performance. Self-aligned SiGe process flows coupled with the elevated Ge content, high doping concentrations, and reduced device dimensions envisioned through technology scaling has led to the dramatic improvements in dynamic performance (i.e., f_T and f_{MAX}). Fig. 6.2 provides an overview of peak f_T and f_{MAX} published in the literature over the past 10+ years, where modern SiGe HBTs exhibit a 7× improvement over early technologies.

While the total ionizing dose (TID) and single-event response of SiGe HBTs have been extensively addressed in previous investigations [87], the impact of technology scaling (i.e., changes to lithographic dimensions, doping concentrations, Ge profiles, etc.) on the overall transient response of these devices is still poorly understood. Fig. 6.3 provides an expanded cross-section of a SiGe HBT, showcasing the internal parasitics influenced by technology scaling. As modern SiGe platforms incorporate novel device topologies and modified processing steps, it is pertinent to understand

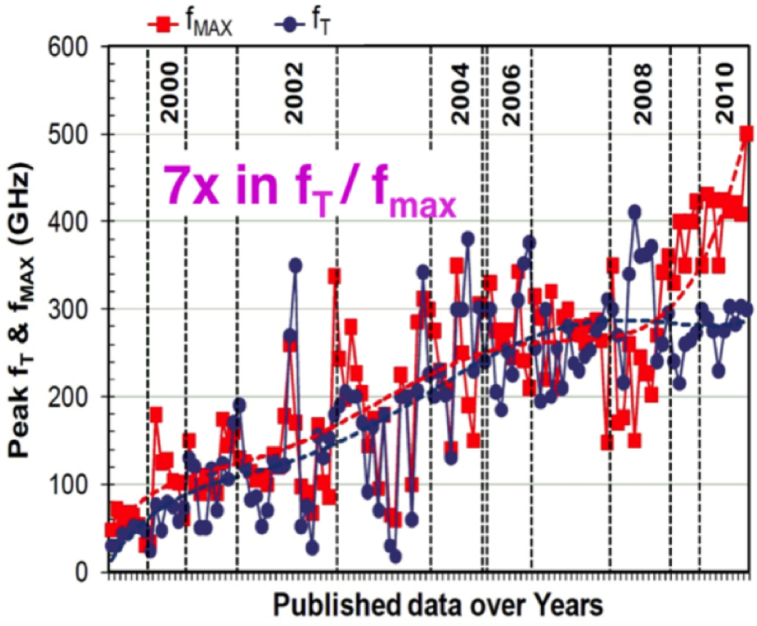


Figure 6.2: Published data on peak f_T and f_{MAX} for various SiGe HBT technologies in the literature.

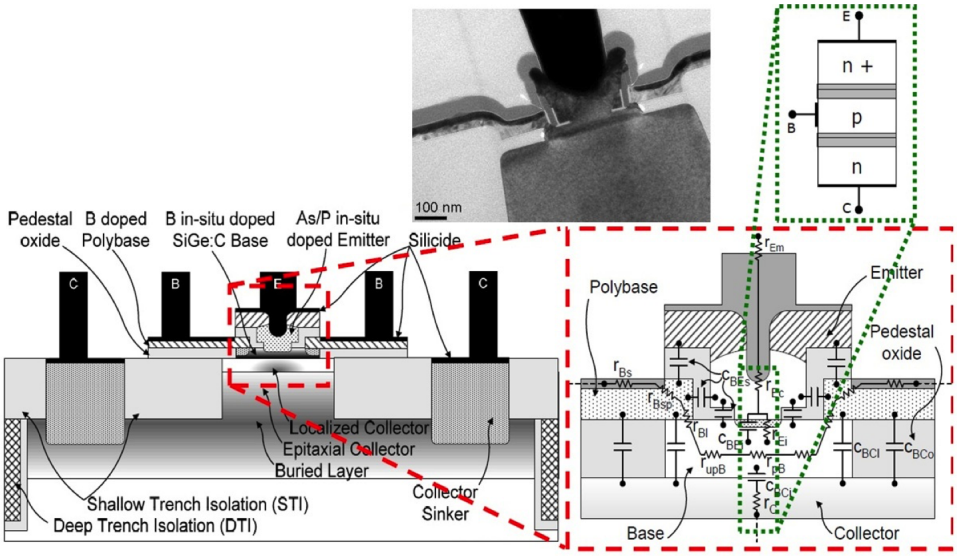


Figure 6.3: Schematic cross-section of a SiGe HBT with an overlay of key intrinsic and extrinsic device parasitics (courtesy of P. Chevalier).

how these changes will affect single-event effect (SEE) sensitivity. Therefore, the present investigation has three major goals: 1) to characterize the transient response of SiGe HBTs across multiple technology generations (this has never been done), 2) to assess current radiation modeling techniques with respect to technology scaling and device biasing, and 3) to determine the primary factors affecting SEE within these devices and provide possible trends for future SiGe BiCMOS technologies.

6.2 Experimental Details

In order to investigate the potential impact of technology scaling on SEE, single SiGe HBT test structures were designed and packaged for transient analysis. Three distinct generations of GlobalFoundries' (formerly IBM Microelectronics) SiGe BiCMOS processes (IBM 5AM (0.5 μm), 8HP (0.13 μm), 9HP (0.1 μm)) were selected for characterization, since these platforms capture a majority of the novel process strategies developed between early, first-generation and current, fourth-generation SiGe BiCMOS technologies [13, 79, 128]. Relevant device parameters for these three technologies are highlighted in Table 6.1. In addition to the large lithographic (lateral) scaling differences between these devices, changes in the device architecture (doping concentrations, Ge profiles, extrinsic regions, metalization, etc.) have strong impact on *dc* and *ac* performance (e.g., breakdown voltage (BV_{CEO} and BV_{CBO}), unity-gain cutoff frequency (f_T), and maximum oscillation frequency (f_{MAX})).

Laser-induced transients on single devices were measured at the Naval Research Laboratory (NRL) using carrier injection by through-wafer, two-photon absorption (TPA). For all 2-D raster measurements, data were collected with a step size of 0.2 μm, unless otherwise noted. To extend this transient analysis to the circuit level, 16-bit digital shift registers utilizing a standard master/slave architecture were designed using the 5AM and 9HP SiGe BiCMOS processes. Both shift registers incorporated an RHBD gated-feedback cell (GFC) clock tree to decouple clock-derived multiple

Table 6.1: Key technology parameters for three generations of GlobalFoundries' (IBM's) SiGe BiCMOS process.

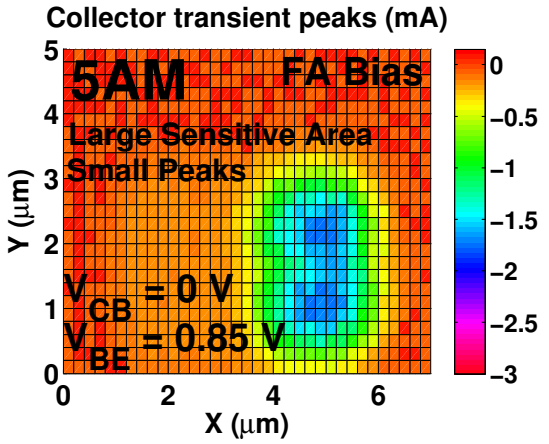
Parameter	5AM [128]	8HP [79]	9HP [13]
Technology Generation	First	Third	Fourth
Drawn Emitter Length (nm)	500	130	100
Effective Emitter Length (nm)	420	120	90
NPN Peak f_T (GHz)	50	200	300
NPN Peak f_{MAX} (GHz)	65	270	350
NPN BV_{CEO} (V)	3.3	1.7	1.7
NPN BV_{CBO} (V)	10.5	5.5	5.2

bit upsets (MBUs) from the overall circuit-level SEE response. These shift registers were taken to the BASE facility at LBNL and irradiated using a heavy-ion cocktail across multiple linear energy transfers (LETs), where bit-error-rate testing (BERT) was performed using an Agilent MP1764 pattern generator and error detector. The current densities within each shift register were selected to provide the fastest switching speeds (i.e., current density near peak f_T). All comparisons are done at a data rate of 1 Gbps, unless otherwise noted. Expanded descriptions for the heavy-ion broad-beam and pulsed-laser experiments have been provided in Section 3.3 and Section 3.4, respectively. The reader is directed there for more information.

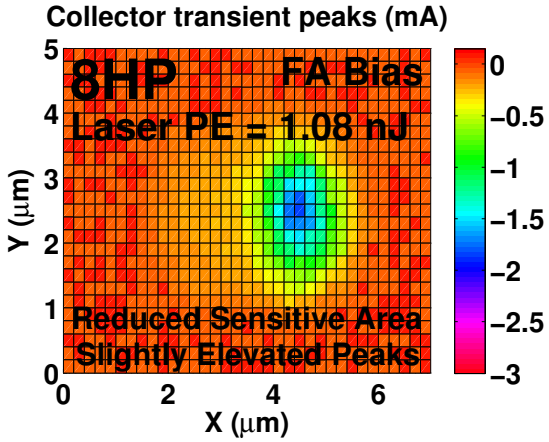
6.3 Experimental Results

6.3.1 Pulsed-Laser TPA Testing

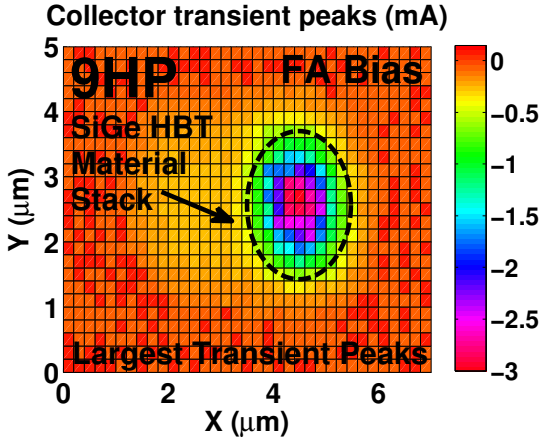
2-D raster scans detailing the laser-induced collector transient peaks for all three SiGe HBTS are shown in Fig. 6.4 under a forward-active (FA) bias (i.e., emitter-base junction forward-biased, collector-base junction reverse-biased). All devices were biased to a steady-state collector current density near peak-f_T, a relevant operating regime commonly encountered in many high-performance RF and bipolar logic applications. The minimum and maximum color map extrema have been matched to improve subsequent device-to-device comparisons. The first-generation SiGe HBT (5AM) exhibits



(a)



(b)

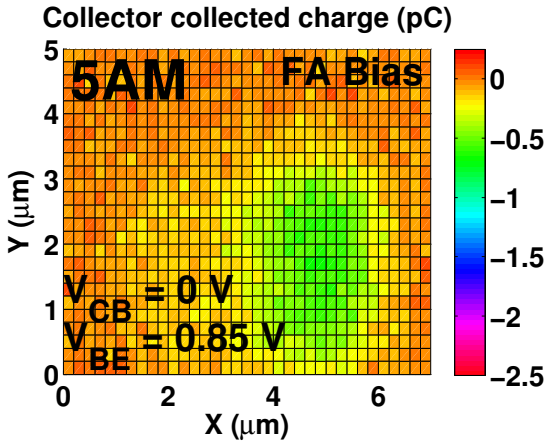


(c)

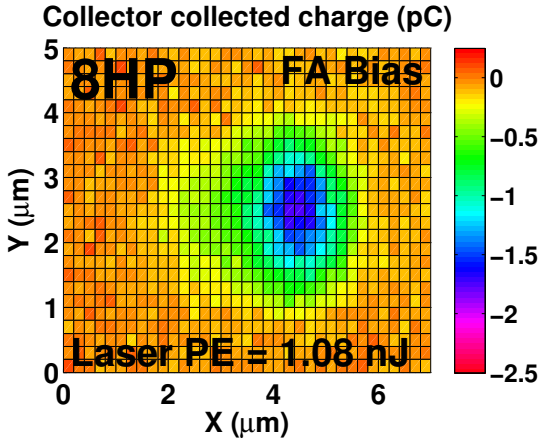
Figure 6.4: 2-D raster scan maps detailing the collector transient peaks for three generations of SiGe HBTs under a forward-active bias ($V_{BE} = 0.85\ V$, $V_{CB} = 0\ V$). (a) IBM 5AM (0.50 μm), (b) 8HP (0.13 μm), and (c) 9HP (0.10 μm).

a larger sensitive area compared to third-generation (8HP) and fourth-generation (9HP) devices due to the increased lateral dimensions of the intrinsic and extrinsic device area. However, when comparing the regions corresponding to the SiGe HBT material stack (emitter/base/collector) between 5AM (Fig. 6.4(a)), 8HP (Fig. 6.4(b)), 9HP (Fig. 6.4(c)), the peak transient magnitude is shown to increase with technology scaling. By integrating the current transient waveforms with respect to time, 2-D maps detailing the collected charge are obtained, as shown in Fig. 6.5(a) through Fig. 6.5(c). These measurements indicate that newer, highly-scaled SiGe generations are more effectively collecting radiation-induced charge carriers, with the 9HP device collecting approximately 39% and 264% more charge than 8HP and 5AM, respectively. These observations suggest that scaling-induced changes, such as doping concentrations and Ge content, may actually degrade the SEE response of current and future SiGe BiCMOS technologies. This result is clearly of significance to the radiation effects community.

Time-domain transient waveforms for the three SiGe platforms are shown in Fig. 6.6. While the 5AM HBT does exhibit a transient peak between the collector, base, and emitter terminals, 8HP and 9HP HBTs exhibit an increased peak transient magnitude, wider pulse width (FWHM), and a large diffusion component between the collector and emitter terminals. These transient signatures agree with previous 2-D raster scans and indicate that the collector-emitter diffusive component is accounting for the majority of collected charge in modern SiGe HBTs under forward-active bias.



(a)



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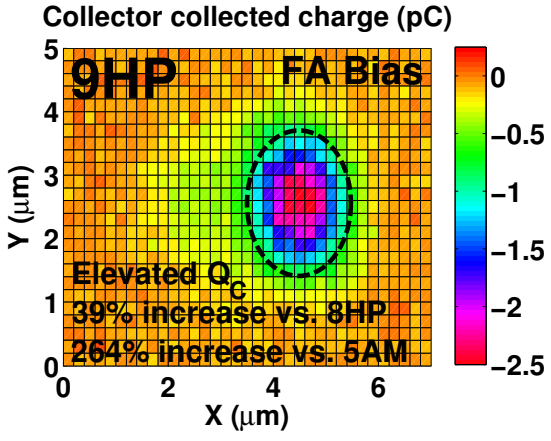

(c)

Figure 6.5: 2-D raster scan maps detailing collected charge at the collector terminal for three generations of SiGe HBTs under a forward-active bias ($V_{BE} = 0.85\ V$, $V_{CB} = 0\ V$). (a) IBM 5AM (0.50 μm), (b) 8HP (0.13 μm), and (c) 9HP (0.10 μm).

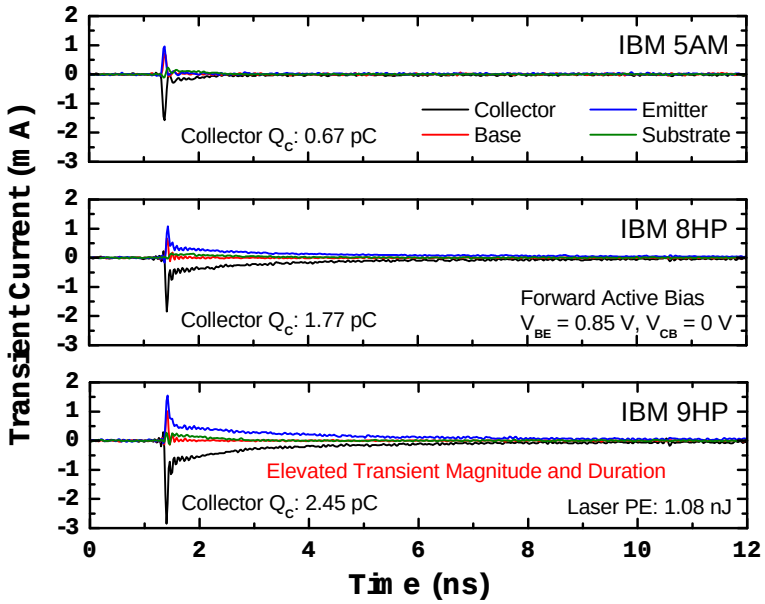

Figure 6.6: Measured collector current transients for the 5AM (0.5x1 μm^2), 8HP (0.13x1 μm^2), and 9HP (0.1x1 μm^2) SiGe HBT under a forward-active bias ($V_{BE} = 0.85\ V$, $V_{CB} = 0\ V$) and a laser pulse energy of 1.08 nJ.

6.3.2 Heavy-Ion Broad-Beam Testing

The measured 1 Gbps bit-error rate (BERT) cross-sections for the 5AM and 9HP-based 16-bit shift registers are shown in the upper plot of Fig. 6.7. While the 5AM digital structures exhibited a higher saturated cross-section, it is important to note that these broad-beam signatures do not take into account the large differences in sensitive area between first-generation and fourth-generation SiGe HBTs, as was shown in Fig. 6.4. Therefore, modified error cross-sections were calculated by normalizing the broad-beam data to the appropriate lithographic dimensions (emitter stripe area) of the SiGe HBTs utilized in each design. For the 5AM shift register, the total emitter area (i.e., all D-flip-flops, clock buffers, and input/output data buffers) was 3.4955×10^{-10} μm^2 (3.4955×10^{-18} cm^2), while the total emitter area for the 9HP design was approximately one order of magnitude smaller at 3.4×10^{-11} μm^2 (3.4×10^{-19} cm^2). The normalized error cross-sections in Fig. 6.7 show that the 9HP

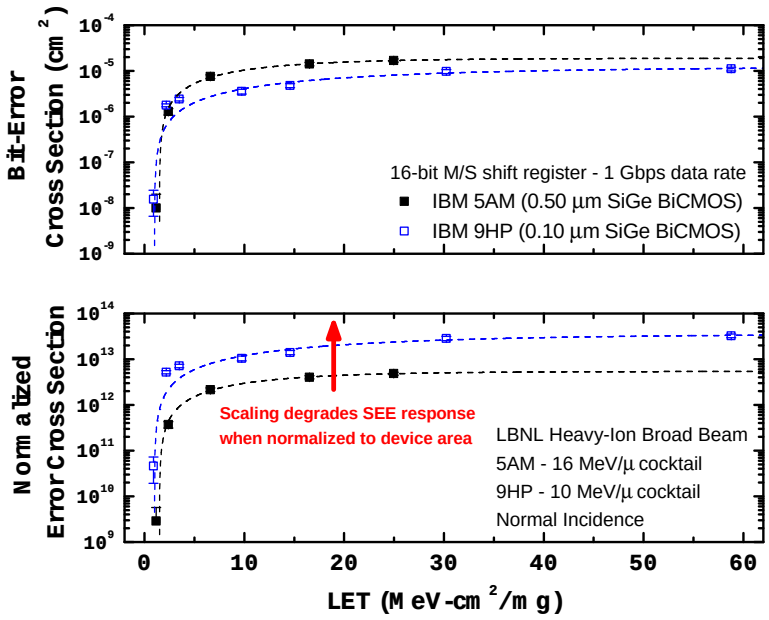

Figure 6.7: Measured and normalized bit-error cross-sections for the 5AM and 9HP 16-bit shift registers operating at 1 Gbps data rate as a function of LET.

shift registers are inherently more susceptible to SEE across all ion-strike LET, providing a confirmation to previous device-level TPA results that technology scaling may increase device sensitivity to SEE.

6.4 3-D TCAD Modeling

To provide a deeper understanding of the underlying mechanisms responsible for the observed SEE scaling dependencies under pulsed-laser TPA and heavy-ion broad-beam testing, a 3-D TCAD model deck for a *npn* SiGe HBT was developed using CFD Research Corporation's nanoTCAD software suite [103]. Within this simulation framework, the vertical profile (i.e., doping concentrations, base width, and Ge profile, etc.) and lateral profile (i.e., extrinsic device regions) can be modified to assess their impact on device transient response. All ion-strike simulations are assumed to be normal to emitter-center, unless stated otherwise. The ion-track depth was set to 11 μm to ensure sufficient charge deposition throughout all sensitive volumes. Ion-strike transient simulations were performed across multiple linear energy transfers

(LETs), though to simplify the present discussion all simulations are for a heavy-ion strike with an LET = 1 MeV-cm^2/mg.

Fig. 6.8 shows the changes in the collector transient waveform across multiple Ge profiles (15% to 29% peak Ge). As the peak Ge content in the SiGe base is increased, the peak transient magnitude, pulse width (FWHM), and transient duration are shown to monotonically increase. The peak magnitudes (in mA), pulse width and transient duration (in ps) for each ion strike were extracted and overlaid against peak Ge content, resulting in the plot shown in Fig. 6.9. Classically, as SiGe BiCMOS processes scale towards smaller lithographic nodes, Ge content is increased to boost the Ge-induced electric field and facilitate faster minority carrier transport across the neutral base region, thereby increasing f_T and f_{MAX}. Therefore, from Fig. 6.9 it is evident that the Ge content is one of the major driving forces affecting the SEE response of SiGe HBTs, possibly due to greater charge separation from the Ge-induced conduction band bending and elevated electric fields present in the base region. While SEE-induced electrons easily drift between emitter and collector due to these elevated

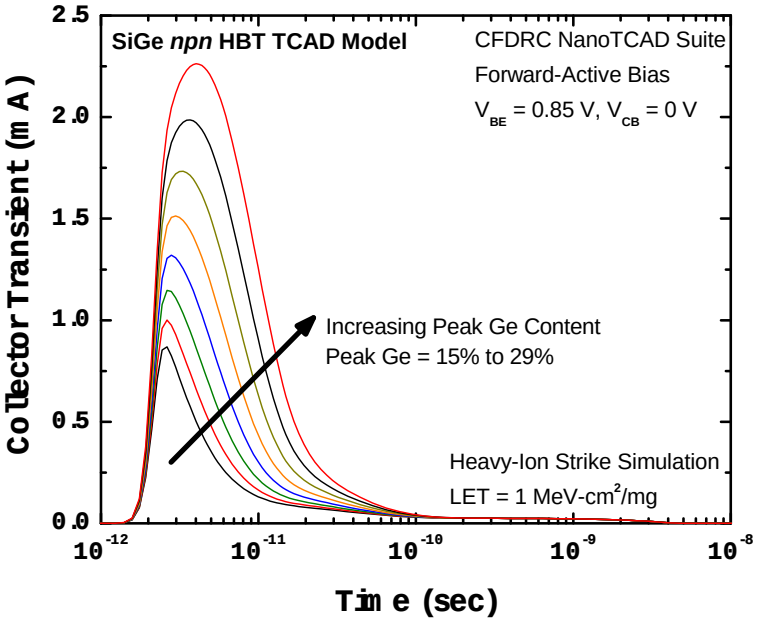

Figure 6.8: Simulated collector transients for an LET = 1 MeV-cm^2/mg ion strike across peak Ge content (15% to 29%).

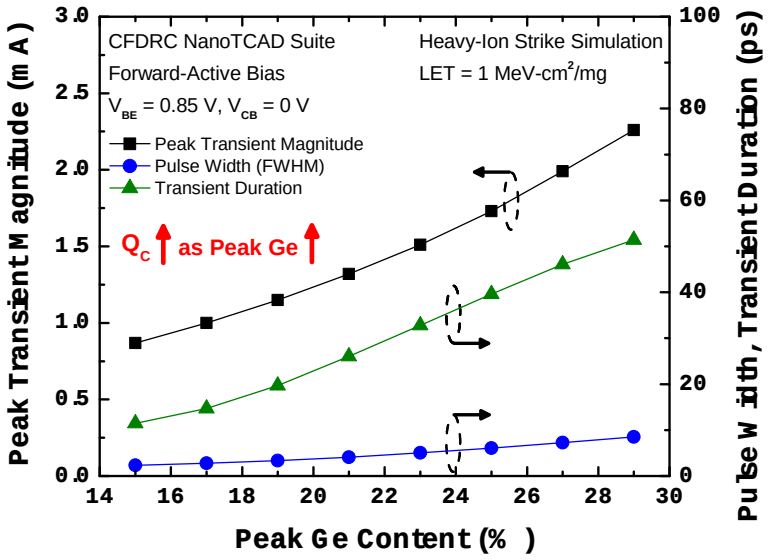

Figure 6.9: Peak transient magnitude, pulse width, and transient duration across peak Ge content for an LET = 1 MeV-cm^2/mg ion strike.

electric fields, the build up of holes in the base region are able to back inject into the emitter, thereby producing a large increase in emitter-to-collector current. This bipolar transient effect may be responsible for the large diffusive component seen in Fig. 6.6 for the 8HP and 9HP SiGe HBTs.

In addition to the Ge profile, the doping level of the selectively-implanted collector (SIC) has significant implications on device performance. For high-performance SiGe HBTs, it is common to have multiple phosphorous implants in the intrinsic collector region, resulting in elevated doping concentrations that delay Kirk and barrier effects and thus improve dynamic performance. From Fig. 6.10, increased SIC doping appears to slightly reduce the peak transient magnitude, but has minimal impact on pulse width and transient duration. The experimental and TCAD results presented here suggest that SiGe technology scaling may have a strong impact on the radiation-induced transient response of SiGe HBTs, with future SiGe technology generations potentially exhibiting increased sensitivities to SEE.

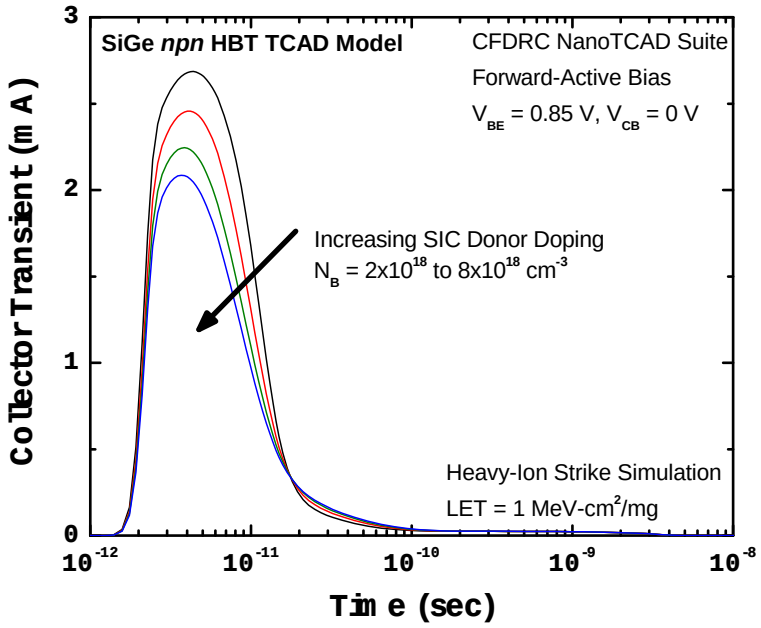

Figure 6.10: Simulated collector transients for an LET = 1 MeV-cm^2/mg ion strike across SIC doping level ($2\times10^{18} - 8\times10^{18}$ cm^{-3}).

6.5 Summary

Pulsed-laser TPA and heavy-ion broad-beam testing of SiGe HBT device and digital test structures are utilized to investigate the potential impacts of semiconductor process scaling (i.e., lateral/vertical scaling, changes in doping, Ge content, etc.) on the overall SEE response of SiGe BiCMOS technologies. These preliminary results show that SiGe technology scaling may have a strong impact on the radiation-induced transient response of SiGe HBTs, with future SiGe technology generations potentially exhibiting increased sensitivities.

CHAPTER 7

CONCLUSION

7.1 Summary of Contributions

This work explores radiation-induced transient phenomena within silicon-germanium heterojunction technologies. While SiGe HBTs exhibit multi-Mrad TID hardness, their susceptibility to SEE remains a primary concern for long-term operation within extreme environments. Therefore, the ability to implement low-overhead solutions that provide enhanced radiation tolerance at a low cost is highly desirable in the radiation effects community. The specific contributions of this work include:

1. An analysis on the TID response of a modern, fourth-generation, 90 nm SiGe BiCMOS technology. These devices maintain the robustness previously exhibited by third-generation SiGe HBTs, which is attributed to the "raised extrinsic base" architecture, a necessary process innovation in high-performance SiGe platforms.

2. The demonstration of inverse-mode biasing as an effective SEE mitigation technique within bulk, silicon-based technologies. The improved isolation between the IM electrical collector (physical emitter) from the thick silicon substrate resulted in a sharp decrease in sensitive area, transient peak magnitude, and transient duration.

3. The design of > 1.0 Gbps inverse-mode, SiGe-based bipolar logic. In addition to the aforementioned enhanced radiation response, modern SiGe BiCMOS HBTs operating in inverse mode provide sufficient *dc* and *ac* performance for high-speed digital, precision analog, and RF applications.

4. An analysis on the transient response of a state-of-the-art, complementary SiGe BiCMOS technology. Bulk *pnp* SiGe HBTs demonstrate a superior SEE response (reduced sensitive area, peak transient magnitude, pulse width, and transient duration) over standard *npn* devices due to presence of an n-well isolation layer.

5. The expansion of circuit-level, mixed-mode analyses to high-frequency RF applications. These simulations show that current modeling approaches are capable of capturing the transient phenomena within RF circuits and indicate that packaging parasitics, in addition to device calibration, have powerful implications on simulation fidelity.

6. An analysis on the effects of semiconductor technology scaling with respect to the transient response of SiGe technologies, where modern devices demonstrate increased sensitivities to SEE due to process changes (e.g., lateral/vertical scaling, differences in doping concentration, novel Ge profiles, etc.).

7.2 Future Work

There are several extensions of this research that are exciting research topics.

1. While device-level results suggest that inverse-mode SiGe HBTs provide a benefit with respect to a circuit's radiation response, high-frequency benchmark circuits (e.g., mixer, PLL, receiver/transceiver, etc.) can be designed to further analyze the tradeoffs between circuit performance and mitigation of single-event effects (SEE).

2. The are significant research opportunities for circuit applications utilizing *pnp* SiGe HBTs. The impact of *pnp* HBTs on the circuit-level response to single-event transients (SET) is still poorly understood.

3. Adapting current radiation modeling techniques (e.g., CFDRC NanoTCAD and Synopsys Sentaurus Workbench) to accurately capture the radiation-induced transient phenomena within high-frequency circuits and sub-systems.

4. Investigating the impact of total dose damage (i.e., interface traps, mobility degradation, etc.) on the transient response of SiGe HBTs.

5. Analyzing the differences between heavy-ion and pulsed-laser-induced SET waveforms and expanding the ability for 2-D and 3-D TCAD models to reliably model these radiation events.

6. Investigating the *dc* and *ac* performance of modern, complementary SiGe BiCMOS (C-SiGe BiCMOS) platforms down to deep-cryogenic temperatures to capture the performance trends between *npn* and *pnp* SiGe HBTs.

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